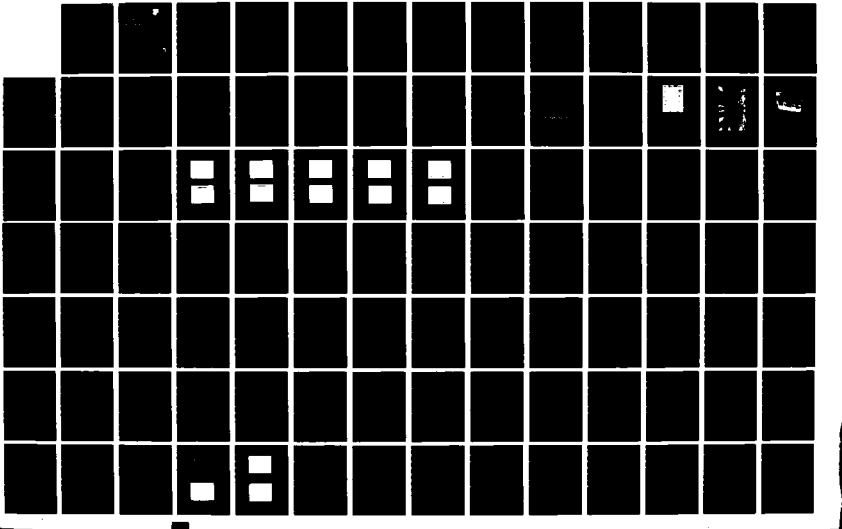
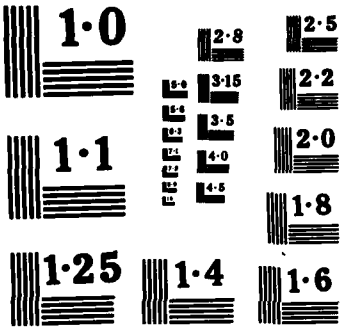
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In-House Report
June 1985

EVALUATION OF THE USE OF p-n STRUCTURES AS PHOTODETECTORS IN SILICON INTEGRATED CIRCUITS

Charles A. Eldering, 1/Lt, USAF

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The light sensitivity of p-n junctions in silicon integrated circuits has been investigated, and the spectral and temporal response of several structures in an integrated circuit measured. A model for the spectral response was developed based on models previously used to study solar cell response. This model takes into account the depth and the active area of the carrier collecting junction and demonstrates the shifting of the peak spectral response towards shorter wavelengths as junction depth and active area decreases. Measurements of the spectral response of junctions in an integrated circuit were compared with the predicted responses. An investigation into the temporal response of p-n photodiodes has shown that the response time of the diode is dependent on both the geometry of the junction and the wavelength of light generating the carriers. Response times for structures in the integrated circuit were measured using a He-Ne laser operating at 0.632 um.

This report provides information which may be useful in developing very large scale

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integrated (VLSI) circuits with integrated photodetectors. Integrated photodetectors are seen to have applications in the laser testing of integrated circuits and development of optically interconnected devices.

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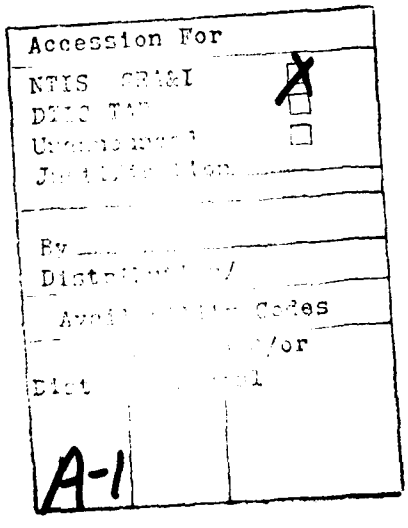




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LIST OF SYMBOLS

$A_{(n)}$	active area of region (n) in diode
D_n	diffusion coefficient of electrons in p-type material
D_p	diffusion coefficient of holes in n-type material
E	electric field
E_G	bandgap energy (indirect)
E_{DR}	bandgap energy (direct)
$F(\lambda)$	incident photon density per second per unit bandwidth at wavelength λ
G	carrier generation rate due to incident light
J	current density
$J_{(n)}$	current density contribution from region (n) in diode
L_n	electron diffusion length in p-type material
L_p	hole diffusion length in n-type material
n	electron concentration
n_p	electron density in p-type material
n_{po}	electron density in equilibrium
p	hole concentration
p_n	hole density in n-type material
p_{no}	hole density in equilibrium
q	electronic charge
QE	quantum efficiency
S_n	surface recombination velocity for electrons
S_p	surface recombination velocity for holes
T	total wafer thickness
T'	wafer thickness minus junction depth and depletion region thickness
V_d	built-in voltage
V_o	self-depletion bias

V_R applied reverse bias

W total depletion region width

W_n depletion region width on n-side of junction

W_p depletion region width on p-side of junction

x_j distance from surface to junction (junction depth)

x_n distance from surface to depletion region edge in n-material

x_p distance from surface to depletion region edge in p-material

$\alpha(\lambda)$ wavelength dependent absorption coefficient

λ wavelength

ρ resistivity

τ_c charge collection time

τ_d diffusion time

τ_p electron lifetime in p-material

τ_{RC} RC time constant

τ_r photodiode rise time

μ_p electron mobility in p-type material

μ_n hole mobility in n-type material

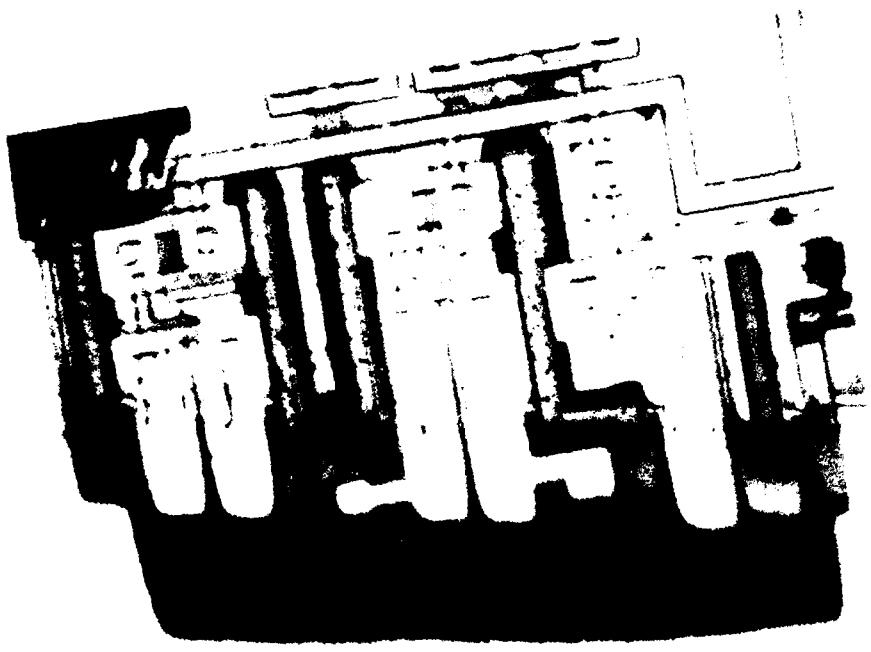


Figure 2.6. Angle-lapped and stained region of the device. p-well is stained dark in contrast to the n-substrate and n^+-contacts which appear light. n^+-contacts are visible at the edges of the well region.

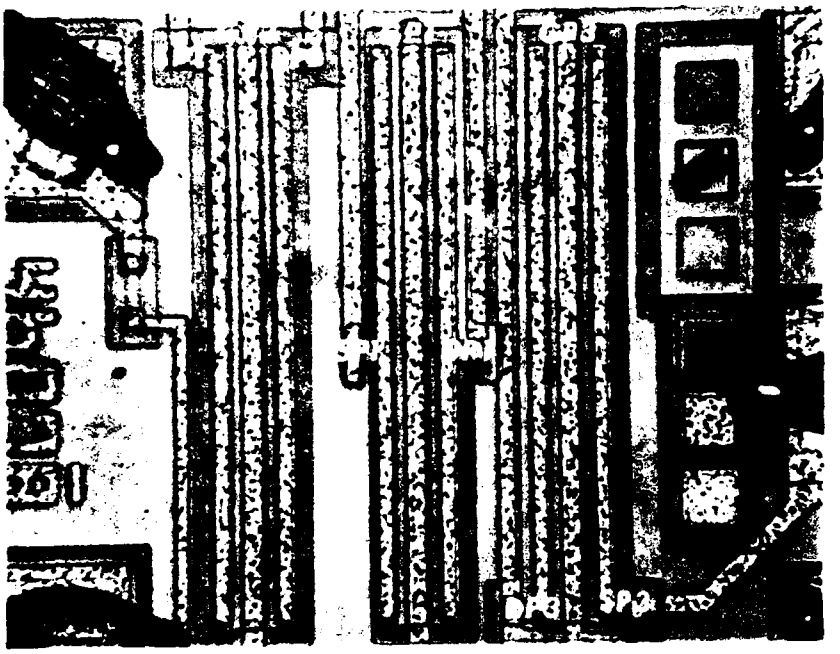


Figure 2.4. p-type transistors with gate, drain, and source contacts labeled.

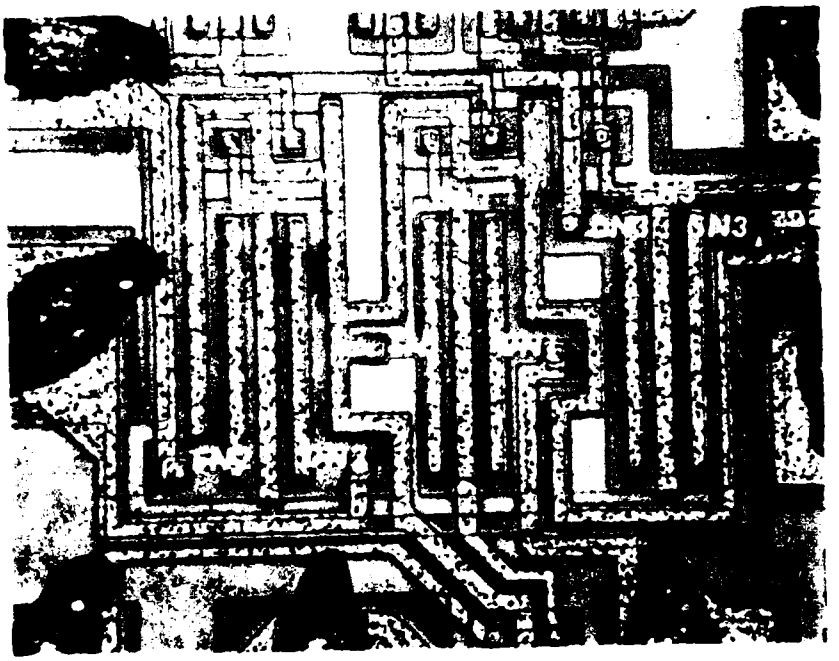


Figure 2.5. n-type transistors with gate, drain, and source contacts labeled.

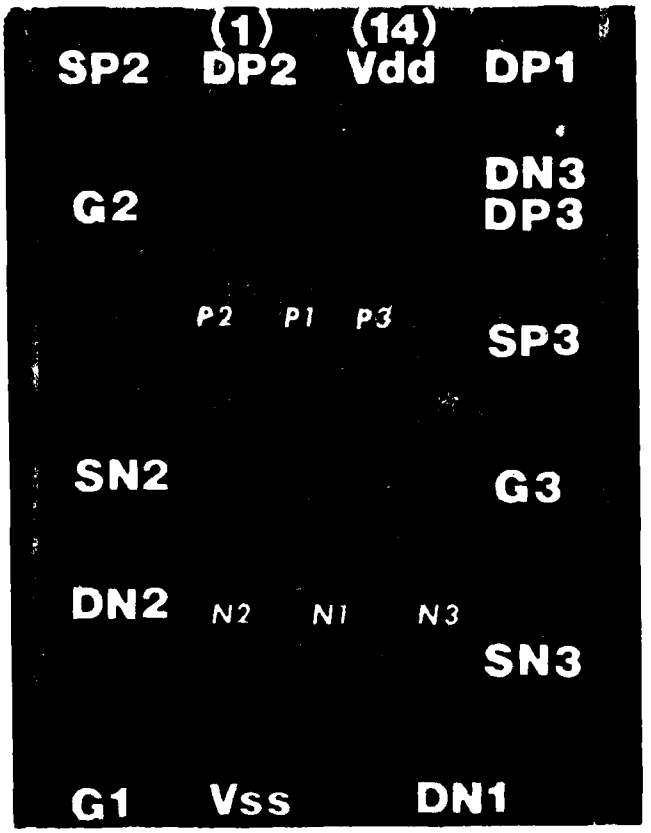


Figure 2.3. Photomicrograph of the 4007 with n-type and p-type transistors labeled. Die size is approximately 32 x 62 mils.

2.2 PHYSICAL LAYOUT AND ANALYSIS OF THE 4007.

A photomicrograph of the 4007 is shown in Figure 2.3. The external pin connections and the p-type and n-type transistors are labeled in correspondence to the electrical diagram in Figure 2.1. Figures 2.4 and 2.5 provide a closer view of the p-type and n-type transistors with their gate, drain and source metallizations labeled.

In order to fully understand the photoresponse of various p-n junctions in the 4007 it was necessary to obtain a good three-dimensional picture of the structures of interest. This was accomplished by combining geometrical measurements of the surface and of an angle-lapped region of the device. The procedure used in angle lapping the device is outlined in Microelectronics Failure Analysis Techniques (43) and consists of removing the device from its package, mounting it on a suitable lapping block and then polishing the device with alumina paste (in this case 3.0 μm rough and then 1.0 μm final) until the region of interest is reached. The device was then stained with a junction delineation p-type stain (Fuller's Stain) consisting of 99.5 parts by volume hydrofloric acid and 0.5 parts by volume nitric acid. Figure 2.6 is a photomicrograph of the n-type transistor region after angle lapping and staining. The p-well region is clearly seen as are the n^+-contacts, and the p^+-contacts into the well region are visible at the edges of the well. Using a Filar eyepiece on a standard metallograph, measurements of the width and length of the diffusions were made. An interferometer was employed to measure the junction depth on the angle-lapped section. This information was recorded and is presented in Table 2.1.

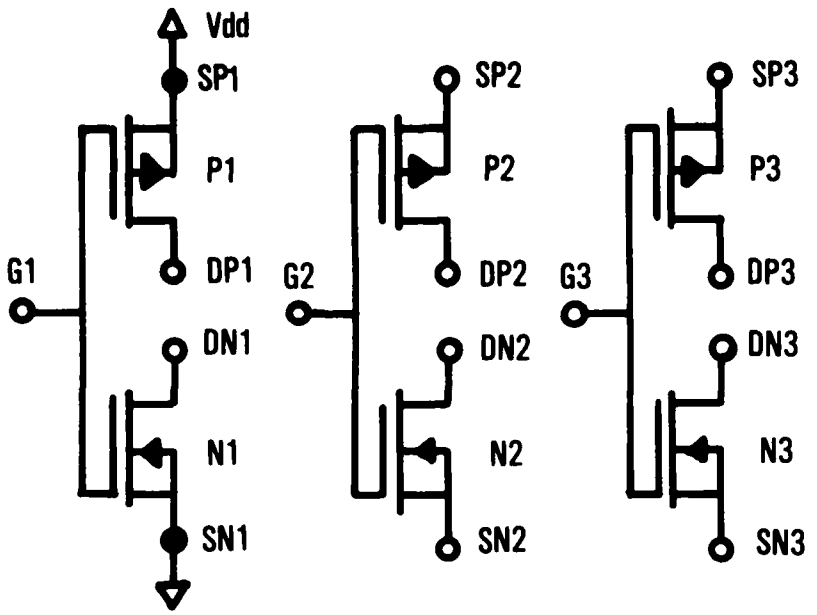


Figure 2.1. Electrical schematic for the 4007 showing gate, drain, and source connections.

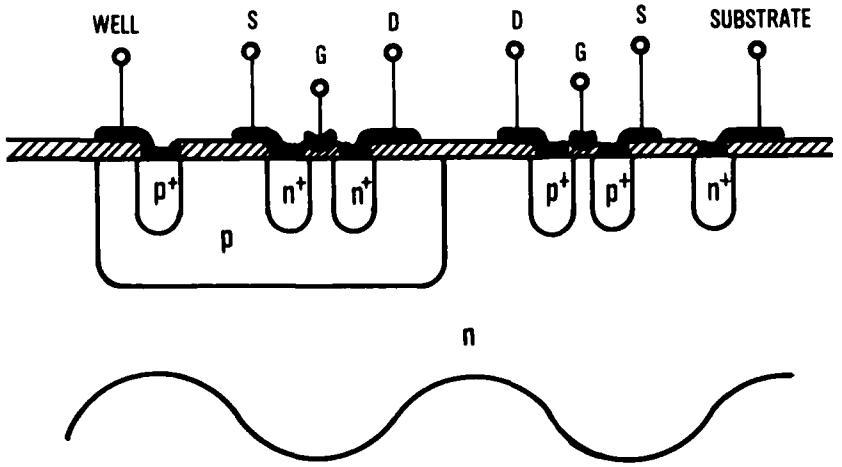


Figure 2.2. Cross section drawing of a typical CMOS device.

2.1.2 CMOS TECHNOLOGY DESCRIPTION.

A general description of the CMOS process was obtained from a text by Glaser and Subak-Sharpe (41) and details for the process used to produce the 4007 were obtained from the manufacturer (42). The process used in fabricating the 4007 utilizes 13 masks and approximately 200 process steps. The process begins with phosphorous doped n-type <111> oriented silicon wafers with a resistivity of 4-6 ohm-cm corresponding to a dopant level of approximately $9x10^{14}$ atoms/cm^3. After field oxide growth and the appropriate masking steps p-wells are created using a boron ion implant and subsequent drive-in. The p-well resistivity is in the range of 3-5 ohm-cm corresponding to a dopant level of approximately $3.5x10^{15}$ atoms/cm^3. The p-well actually has a Gaussian impurity distribution as it is diffused from a finite ion-implanted source. The p^+-source and drain regions are defined by further masking steps and are created using a boron diffusion and drive-in. These diffusions have a error function distribution due to the diffusion from a constant source and have a high dopant density with an average concentration being in the range of $5x10^{16}$ atoms/cm^3. The n^+-source and drain regions are defined similarly and created using a phosphorous diffusion source. They also have an error function impurity distribution and an average dopant density in the range of $1x10^{17}$ atoms/cm^3. Subsequent masking and process steps are used to form the contacts to the gate, drain and source regions of the device and interconnect the transistors. A representative cross section of the device is illustrated in Figure 2.2.

II. CHARACTERIZATION OF THE CMOS 4007.

2.1 DESCRIPTION OF THE 4007.

2.1.1 FUNCTIONAL DESCRIPTION.

The integrated circuit chosen as a test vehicle for this work was the 4007 CMOS dual complementary pair plus inverter. The samples used were manufactured by the National Semiconductor Corporation in 1980. A CMOS device was chosen since CMOS is a popular technology for the fabrication of VLSI devices and is expected to become the predominant technology for the production of all digital Si devices (40). This is due to the low power consumption and high operating speeds which can be obtained using complementary p-type and n-type MOS transistors. The 4007 was selected in particular due to its electrical configuration, as illustrated in Figure 2.1. Three p-type enhancement and three n-type enhancement transistors are provided, some of which have individual connections to the gate, drain, and source contacts. This allowed for direct measurement of many of the electrical characteristics of the integrated transistors and p-n junctions formed in the device, along with the ability to bias the substrate independently of the source or drain. This would not have been possible with most other CMOS devices, and would have necessitated the use of mechanical probes. The repeated use of probes on the device tends to be destructive and also adds unwanted capacitance during AC circuit measurements. The disadvantage in using the 4007 was that the dimensions of the features and the junction depths are not necessarily representative of those found on state-of-the-art VLSI devices. The areas for source and drain contacts on the 4007 are in the range of 3×10^4 μm^2 while for VLSI devices they are at least an order of magnitude less. Junction depths for VLSI devices are also an order of magnitude less than the 2.5 μm deep junctions of the 4007. However, careful development of models which can account for these differences will allow for extension of this work to VLSI type dimensions.

1.3 ORGANIZATION OF THESIS.

This thesis is a combination of both theoretical and experimental work. Chapter II discusses in detail the CMOS integrated circuit which was used as a test vehicle and identifies the p-n structures of interest. The theory of photodiode operation is discussed in Chapter III and the model for spectral response which was developed is presented. Experiments performed on the test vehicle are described and the results presented and compared with predictions in Chapter IV. A general discussion of the results with some observations concerning VLSI devices with integrated photodetectors is also given in Chapter V, with a summary of the work being given in Chapter VI.

1.2.3 VLSI OPTOELECTRONIC DEVICES.

The increasing gate-to-pin count ratio of VLSI devices is evidenced by devices having 64 pins and upwards of 10,000 gates. This steep ratio results in a bottleneck of information flowing both in and out of the device, which in turn leads to performance limitations and an inability to thoroughly characterize and test new devices. The use of optical signals could alleviate this problem and a number of researchers are currently performing work in this area. Goodman et al. have published several articles which discuss the development of advanced optical computing devices along with an effort to develop optical interconnections for VLSI circuits (35,36). The optical systems proposed include integrated transmitters and receivers on Si devices and holographic elements above the devices with the ability to route optical signals to various locations on the device. While some of these goals require major advancements in integrated circuit technology, such as the ability to grow III-V materials on top of Si to make optical emitters, the necessity to integrate photodetectors on VLSI devices is seen as a realizable goal with success depending on the size and the performance of the detectors. Advances have been reported by Boyd in the development of integrated detectors with the novel approach of illuminating a silicon photodetector along a die edge as opposed to illumination from the surface of the device (37). These edge photodetectors are created by a preferential etching process and have surfaces in <111> directions at an angle of 54.7 degrees to the <100> wafer surface. The quantum efficiency at GaAlAs laser wavelengths is much improved over that for similar surface diodes. This is due to the fact that the majority of absorption takes place in the depletion region of these edge illuminated devices. Advances in waveguide technology will also aid in the development of optical interconnects, and a variety of materials are being used in an attempt to develop waveguides which can be integrated with optoelectronic devices (38,39).

circuits. Edwards (26) and Smith (27) proposed the laser testing of integrated circuits in 1977 in two publications which discuss the relative amounts of photocurrent needed to switch elements on digital devices fabricated in several technologies. They were also able to demonstrate the technique on a MOS device using a HeNe laser and electrooptic modulator. A technique for reading the internal states of digital integrated circuits using a laser was developed by Pronobis and Burns in 1982, and involves the injection of current at p-n junctions using a laser while simultaneously monitoring the power supply current (28). Relative amounts of photocurrent observed at the power supply can be used to determine the logic state of the illuminated node. A variation of this technique was used by Burns et al. in 1984 to inject timing faults at internal locations on a device (29). The development of a commercially available laser probe for extracting electrical information indicates that these techniques may be utilized heavily as a product development tool in the future (30). However, the development of these techniques has not included research to determine the spectral and temporal responses of the photocurrent producing junctions. This work attempts to determine at what wavelengths significant amounts of photocurrent can be produced, and what the associated response times are.

Electron beam testing is a parallel technique to photon beam testing as an electron beam can be used to generate significant amounts of current at a p-n junction, through the generation and subsequent collection of minority carriers. Shaver (31,32) and Lukianoff (33) discussed the use of an electron beam for the testing of devices, and Kinch and Pottle (34) developed a detailed procedure for automatic test generation for beam testable devices. This work is generally applicable to the laser as well as electron beam testing of devices.

amplifiers (8). This work is paralleled by work in the construction of GaAs optical receivers, which have limited integration and complexity, but have optimum spectral and temporal responses for use in fiber optic systems (9)-(12). The theory of photodiode operation is discussed in several textbooks, most notably by Sze (13). Spectral response for p-n solar cells is discussed by Sze and also by Hovel (14). The derivations and models in these texts are equally applicable to p-n photodiodes and the models developed in this work are extensions of these with suitable modifications made to consider the small areas and special structures found in p-n photodiodes on integrated circuits. Several publications have discussed the spectral and temporal limitations of photodiodes, and manufacturers of photodetector devices provide some information in their sales literature regarding the theory of photodiode operation (15)-(19).

1.2.2 LASER AND ELECRON BEAM TESTING.

The use of lasers for the production and customization of Si integrated circuits has been described by Smith (20). Laser programming of random access memories to substitute good cells for bad cells has become a common manufacturing practice and compares well with the use of electrically fusible links. The use of a dye laser to form connections on VLSI devices has also been demonstrated (21). The successful use of lasers for permanent circuit modification indicates that optical signal injection may be useful as a production test tool. However, the techniques that have been developed to date have only been for use as as failure analysis and product development tools. A review of the techniques developed is necessary to demonstrate the possible use of integrated photodetectors in the test environment. Light-spot scanning was developed in 1967 by Haberer, who later used the technique to locate surface inversion problems in integrated circuits (22,23). Laser scanners were employed by Burns (24) and Henley (25) to determine latch-up sensitivity of complementary metal-oxide-semiconductor (CMOS) integrated

with predictable spectral and temporal responses. The goal of this work is thus twofold: to provide an evaluation of p-n structures in a particular integrated circuit for use as integrated photodetectors, and to provide the basis for future work which will aid in the development of silicon devices with integrated photodetectors.

1.2 LITERATURE SUMMARY AND RELATED WORK.

1.2.1 SILICON OPTOELECTRONIC DEVICES.

The generation of current in semiconductor diodes using light is a tool which has found wide use and has been of historical significance in semiconductor research. One of the first publications mentioning the use of photocurrent was in 1964 by Goucher et al., who used a 1.85 μm light source to make carrier lifetime measurements in a Ge diode (1). This was followed by work dealing with Si devices which were employed as photodetectors, primarily non-avalanching photodiodes used in the photoconductive mode (2,3). Multiple photodetectors were soon integrated into bulk Si devices, as demonstrated by the Si reversed-biased diodes which were employed in the Vidicon camera reported by Crowell in 1967 (4).

Modern Si photodiodes are available with various spectral responses and speeds, a typical device having a peak spectral response at 0.95 μm and a rise time of 50 ns with a 50 ohm load (5). In general, Si photodiode responsivity extends from the blue region (0.46 μm) to the near infrared region (1.1 μm), making them useful for detection, radiometry, colorimetry and various other light sensing applications. Si photodiodes have been fabricated as components of circuits as evidenced by commercially available photodiode arrays used as imaging devices. These devices are usually self-scanned (by scan circuitry residing on the device), having clock rates as high as 5 MHz, with an integration time of 2 μs per pixel (6). Experimental Si devices include a 27 channel photodiode array with preamplifiers designed to operate at 0.84 μm (7), and photodiodes with integrated transistor

the optical injection of signals using existing junctions in CMOS devices. The possibility of creating specialized detectors in CMOS devices necessitates the study of other p-n (well-substrate) and n-p-n (contact-well-substrate) structures which could be incorporated into the design of logic devices and used specifically for the conversion of optical signals into electrical signals. The spectral and temporal responses of the structures in the test vehicle were studied and an evaluation of the potential use of these structures in several applications was made. These applications include laser testable and optically interconnected devices.

The usefulness of this work is not intended to be limited to the evaluation of one particular CMOS device or process. It is the intent of this work to provide information which can be extended to evaluate the potential use of structures formed in other technologies (bipolar, CMOS on insulator) as integrated photodetectors. A CMOS device was chosen as a test vehicle since it is a common technology for the fabrication of VLSI devices. By attempting to understand the spectral and temporal responses of the structures in the test vehicle and identifying the key parameters which affect these responses, several areas were discovered in which further research is needed. Three models were developed to predict the spectral responses of the integrated circuit structures. The spectral responses and peak responsivities of the structures were experimentally measured and compared to the predicted responses. One of the models developed predicted the experimentally determined spectral response over the entire range measured while the other models were not as accurate. Refinement of the models to include electric field effects due to doping profiles in the semiconductor may be necessary. The study of the temporal responses included only preliminary experimental measurements; time-dependent models need to be developed. Additional research in these areas will enable the eventual design and production of integrated photodetectors

I. INTRODUCTION

1.1 PURPOSE.

The optoelectronic properties of silicon are utilized in a large number of devices, particularly in p-n, p-i-n and avalanche photodiodes. Silicon integrated circuits do not employ these properties for device use, although all p-n junctions in an integrated circuit are light sensitive to some extent. The large number of p-n junctions in an integrated circuit and their widely distributed positions in the circuitry suggest that they might be employed as photodetectors for modulated optical signals. Utilization of these junctions offers the possibility of creating optically testable or optically interconnected very large scale integrated (VLSI) circuits with production and performance advantages over current Si devices which rely exclusively on electrical signals for the transfer of both input and output information. The applications which these junctions can be used in depends greatly on their operating characteristics, and in particular the junction spectral and temporal responses. The junction spectral response is important since different applications will involve incoming optical signals in different regions of the spectrum. The temporal response determines the maximum frequency the junction can be optically modulated at, and thus may be a limiting factor for use in some applications.

In this work the construction of a digital complementary metal-oxide-semiconductor (CMOS) integrated circuit was examined and several structures were identified for possible use as integrated photodetectors. The existing drain-substrate junctions in CMOS devices can serve as photodetectors and be used to convert optical signals into electrical current. The logic state of the output of a CMOS inverter can be switched if the drain of the transistor which in the "off" state is selectively illuminated with sufficient optical intensity. This allows for

TABLE 1

GEOMETRICAL MEASUREMENTS OF THE WELL AND CONTACT REGIONS OF THE 4007.

Region	Length (μm)	Width (μm)	Depth (μm)
p-well	293.7±.9	387.2±.9	6.75±.14
p+-contacts	378.6±.9	29.4±.2	2.43±.14
n+-contacts	179.5±.9	30.8±.2	2.84±.14

2.3 ELECTRICAL CHARACTERIZATION.

2.3.1 p-n JUNCTION CHARACTERISTICS.

The p-n junction characteristics were of primary importance since they are the junctions which were employed as photodiodes in this study. Figures 2.7 and 2.8 illustrate the forward and reverse bias characteristics for the p-well to n-substrate junction. Figures 2.9 and 2.10 illustrate the forward and reverse bias characteristics for a p^+ to n-substrate junction found in the drain of transistor P2. The other five p^+ to n junctions in the p-transistors were found to have nearly identical characteristics except for small variations in the breakdown voltages which are probably due to geometrical differences in the diodes. Figures 2.11 and 2.12 illustrate the forward and reverse bias characteristics of a n^+ to p junction as found in the drain contact to transistor N2. Once again, this is typical of the characteristics of the other five n^+ to p junctions with minor variations in the breakdown voltage being noted.

2.3.2 BIPOLAR TRANSISTOR CHARACTERISTICS.

Both the parasitic vertical and lateral bipolar transistors which exist in the 4007 are inherent to the bulk CMOS process and are generally considered to be a hazard as they provide the means for latch up of the device to occur, often times with catastrophic consequences. The vertical n-p-n bipolar is of interest however, as its characteristics are vastly different than that of the MOS devices and a hybrid MOS/BIPOLAR technology would have many advantages for digital, analog and power devices. Several authors have reported advances in this area (44,45). During some preliminary experimental work on this project, it was observed that the vertical n-p-n transistor could act as a direct amplifier of photocurrent or simply as a phototransistor and it was therefore considered for possible use as a photodetector. The electrical characteristics of a vertical transistor were measured and are illustrated in Figure 2.13. It was noted that the vertical

transistor characteristics varied widely and that current crowding caused a gain rolloff in some of the vertical transistors.

The lateral p-n-p transistor characteristics were measured to determine whether employment of the vertical transistor as an amplifier or phototransistor could lead to latch up in the 4007. Figure 2.14 illustrates the electrical measurements made on the lateral transistor and it can be seen that the gain of this device is low enough that latch up would not be likely to occur, as the gain product of the lateral and vertical transistors is normally less than 1. This is often taken as an indication of latch-up free operation (45). For construction of a new device utilizing vertical bipolars as photodetectors suitable consideration would have to be given to the problem of latch up.

2.3.3 MOS TRANSISTOR CHARACTERISTICS.

In order to study the circuit operation of a CMOS device and to consider the application of photocurrents as digital switches, the characteristics of the p-type and n-type enhancement transistors were recorded as illustrated in Figures 2.15 and 2.16.

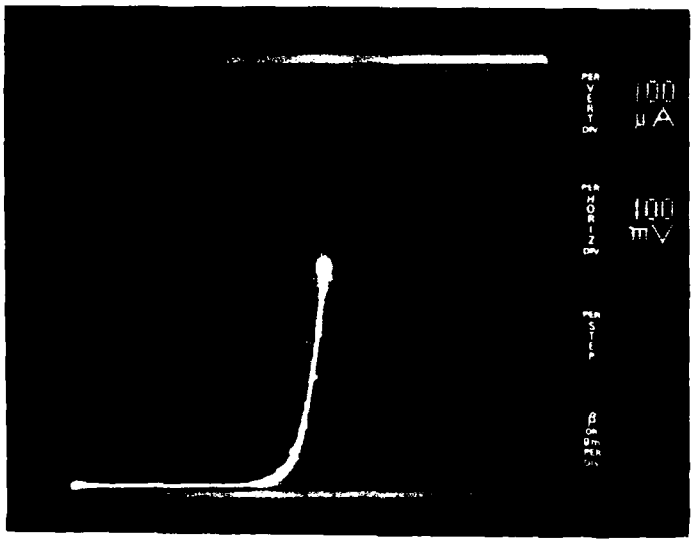


Figure 2.7. Forward bias electrical characteristics of the p-well to n-substrate diode.

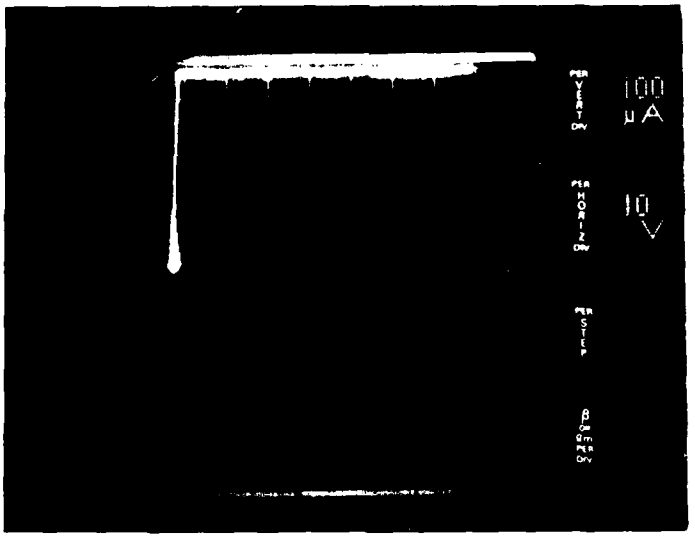


Figure 2.8. Reverse bias electrical characteristics of the p-well to n-substrate diode.

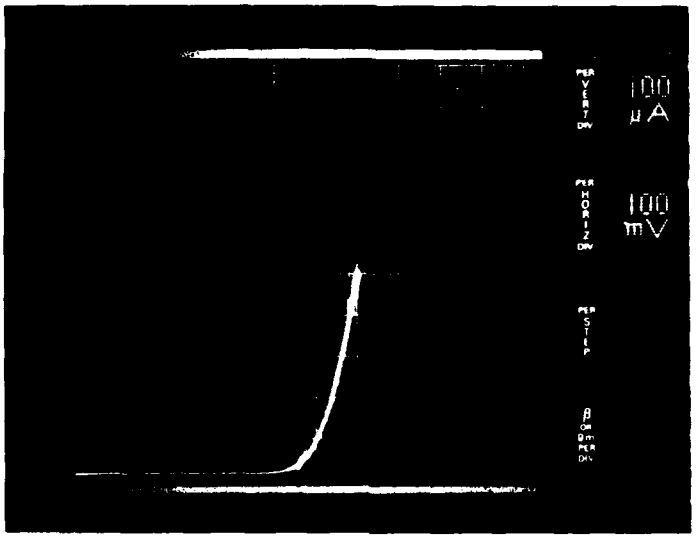


Figure 2.9. Forward bias electrical characteristics of a p^+-contact to n-substrate diode.

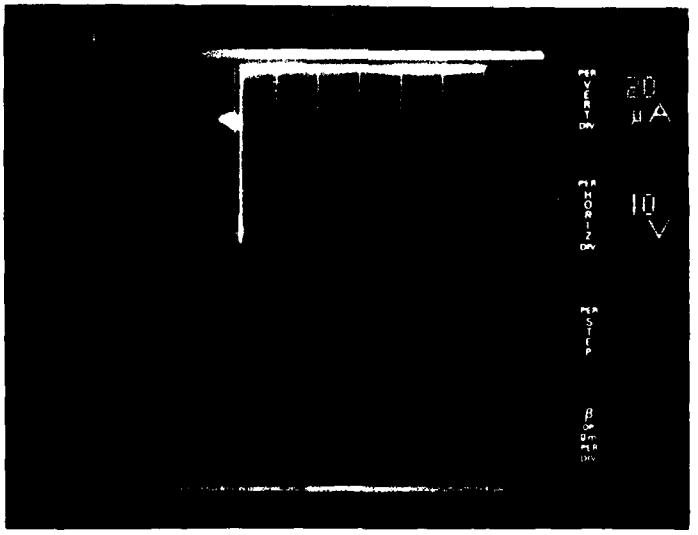


Figure 2.10. Reverse bias electrical characteristics of a p^+-contact to n-substrate diode.

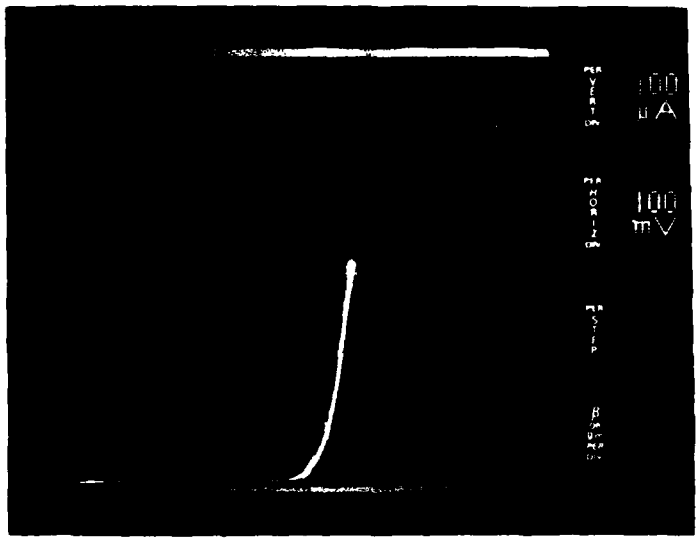


Figure 2.11. Forward bias electrical characteristics of a n^+-contact to p-well diode.

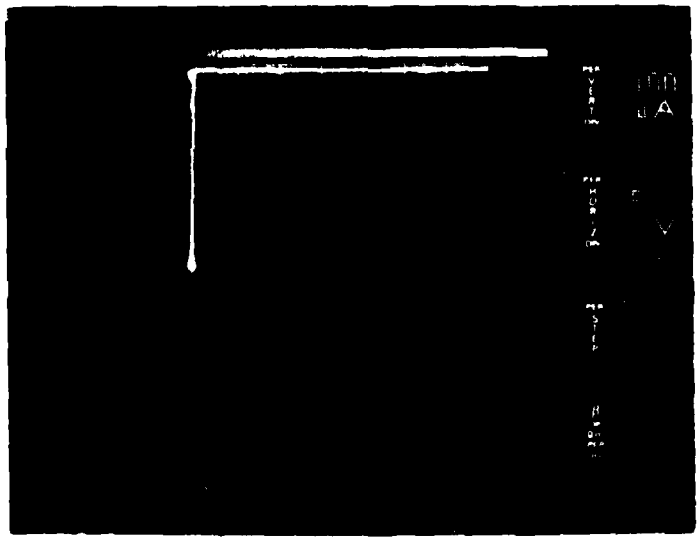


Figure 2.12. Reverse bias electrical characteristics of a n^+-contact to p-well diode.

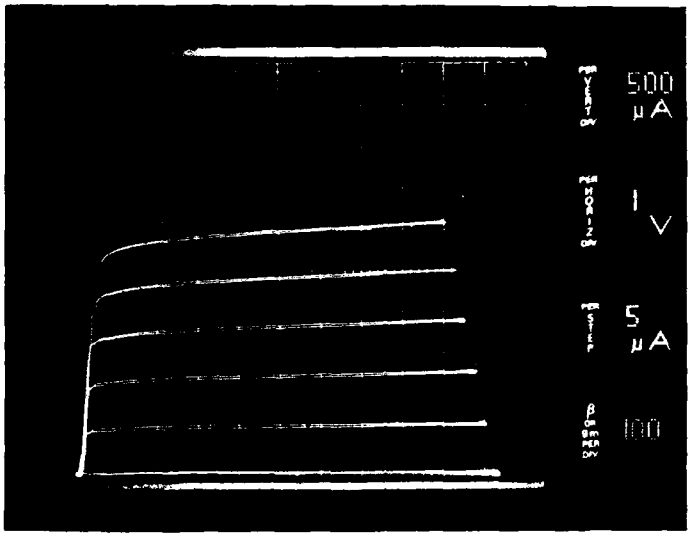


Figure 2.13. Electrical characteristics of a vertical n-p-n transistor.

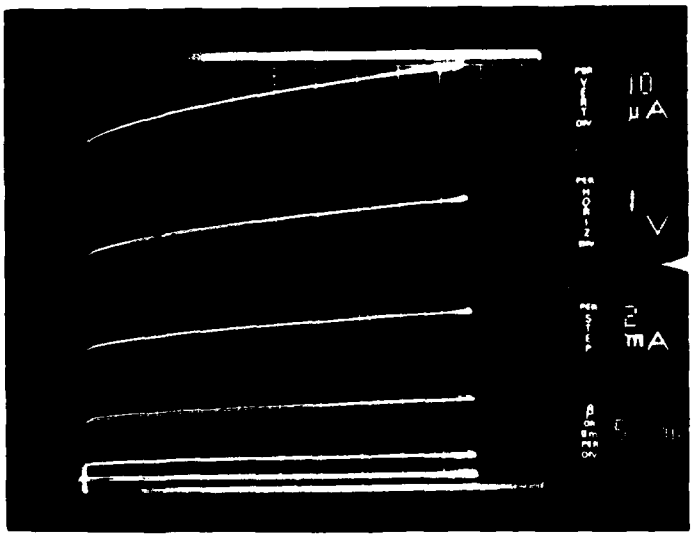


Figure 2.14. Electrical characteristics of a lateral p-n-p transistor.

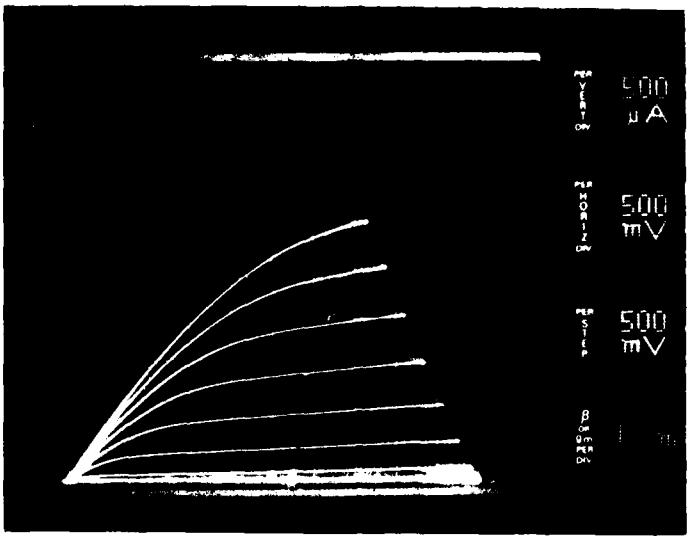


Figure 2.15. Electrical characteristics of a p-channel enhancement MOS transistor.

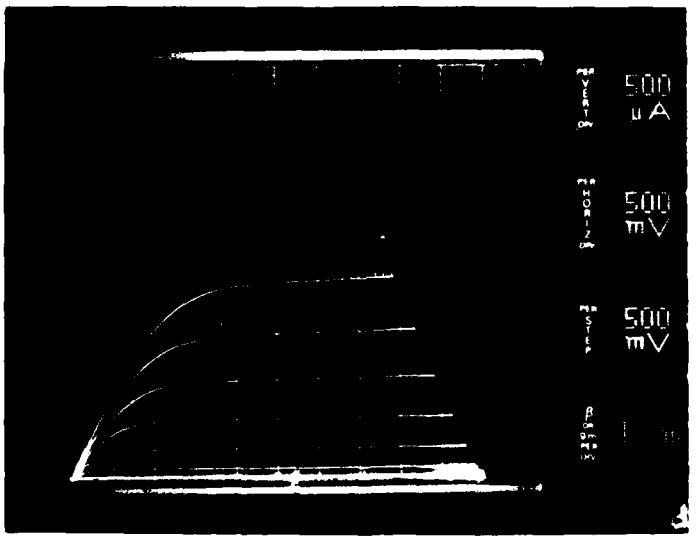


Figure 2.16. Electrical characteristics of a n-channel enhancement MOS transistor.

2.4 IDENTIFICATION OF STRUCTURES OF INTEREST.

Having performed a characterization of the device, it was then possible to identify those structures which might have promise as photodetectors in an integrated circuit. Refering to Figure 2.17, it can be seen that there are three types of p-n junctions formed in the CMOS process which could be used as photodiodes. These junctions are labeled as structures 1, 2, and 3 and will be referred to as such throughout the remainder of this work.

There are two additional structures which were studied for potential as photodetectors and are illustrated in Figure 2.18. Structure 4 is a n-p-n phototransistor which is simply the vertical bipolar transistor with the well-substrate junction being used as the light controlled collector-base junction. Structure 5 is a combination of the photodiode structure 1 and the vertical n-p-n transistor. The transistor provides direct current amplification of the photocurrent generated by the photodiode. This direct amplification capability may allow generation of large enough currents to switch subsequent devices in a circuit.

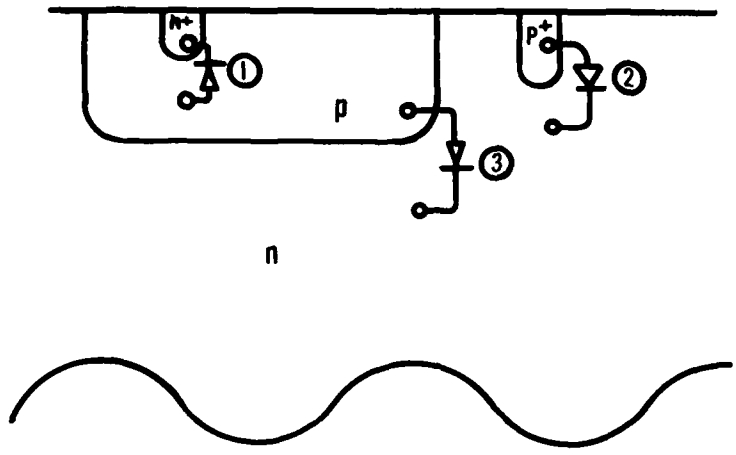


Figure 2.17. The p-n junctions formed in the CMOS process which can be used as photodiodes: structure 1, the n^+-contact to p-well diode; structure 2, the p^+-contact to n-substrate diode; structure 3, the p^+-well to n-substrate diode.

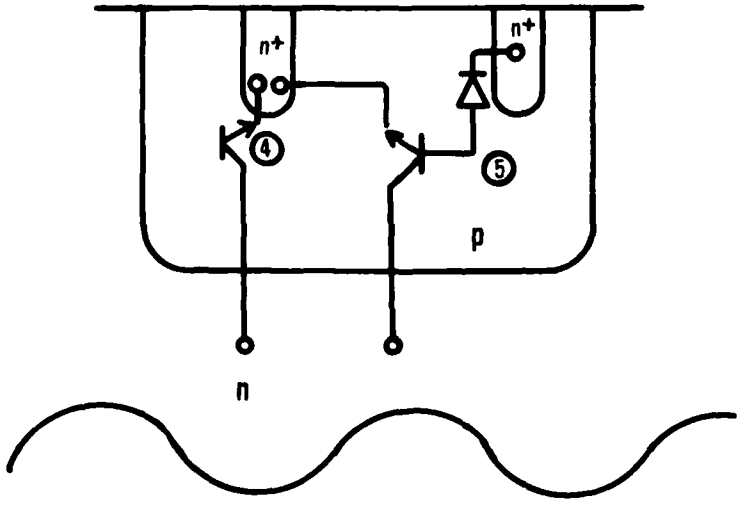


Figure 2.18. Other structures for possible use as photoreceivers: structure 4, the vertical n-p-n transistor which can be employed as a phototransistor with the substrate-well diode being the photocurrent source for the base of the transistor; structure 5, the n-p-n bipolar transistor used as an amplifier for the photocurrent source formed by the n^+-contact to p-well diode.

III. THEORY OF PHOTODIODE OPERATION

3.1 GENERATION AND COLLECTION OF CARRIERS IN SILICON.

The photocurrent produced in an illuminated p-n junction is due to the generation and subsequent collection of free electrons and holes within the semiconductor. By examining the depth dependent generation of carriers and the diffusion of free carriers in a p-n structure, models have been previously developed to predict and understand wavelength dependent photocurrent response. This work extends those models to describe the spectral response of the p-n structures within an integrated circuit.

While optical absorption in Si can result from several processes, the only process which contributes directly to the generation of photocurrent is the excitation of electrons across the gap from the valence band to the conduction band (47). These transitions may be either direct, with no resulting change in the k vector or momentum of the electron, or indirect, in which case the k vector and momentum of the electron are altered. Figure 3.1 illustrates the energy band structure for Si and an indirect transition by absorption of a photon and corresponding emission of a phonon. The conservation of momentum and energy requirements, along with the band structure and phonon spectra determine the absorption characteristics of the material. The absorption coefficient for Si as a function of wavelength is illustrated in Figure 3.2. It is noted that absorption coefficient varies greatly over the range of 0.4 to 1.0 μm, the corresponding 1/e depths being 0.01 and 100 μm respectively. This variation in absorption coefficient as a function of wavelength is of primary importance in determining the spectral response of p-n structures. Reflectance of light from the surface of the Si also plays an important role, as it begins to increase rapidly at wavelengths below 0.6 μm, as illustrated in Figure 3.3.

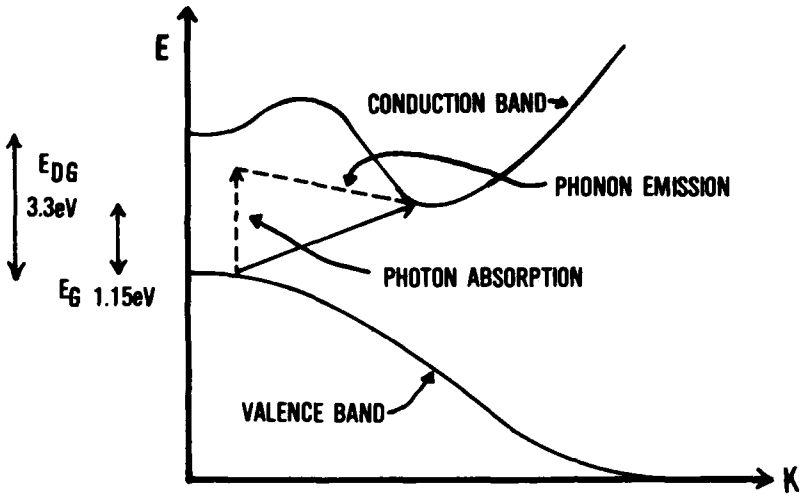


Figure 3.1. Generation of carriers in Si.

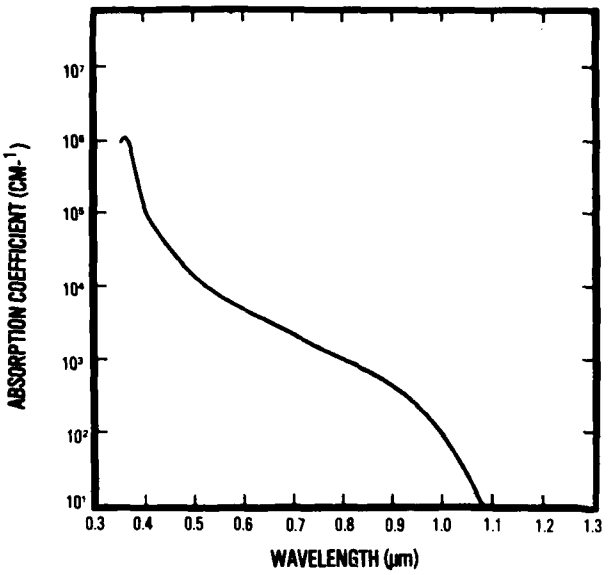


Figure 3.2. Intrinsic absorption coefficient of Si.

Plotted from the data of Jellison and Modine (51).

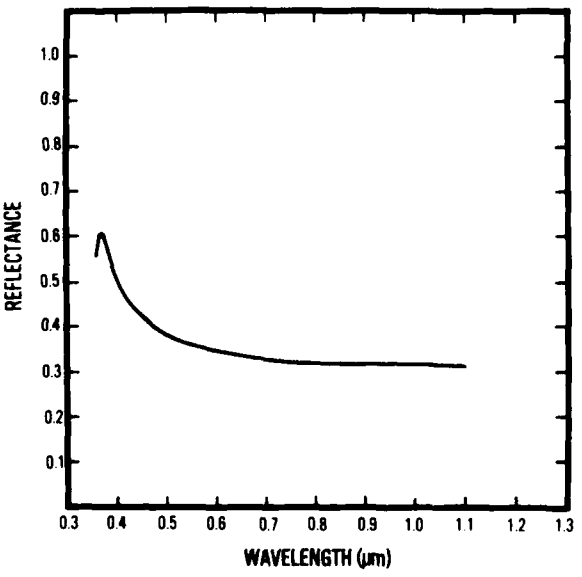


Figure 3.3. Intrinsic reflection coefficient of Si.

Plotted from the data of Jellison and Modine (51).

A typical diffused p-n junction is shown in Figure 3.4, and is representative of the junctions found in solar cells, photodiodes and integrated circuits. Figure 3.5 represents a diffused n-p junction such as is formed in the p-well of a CMOS integrated circuit. In either case, for uniform monochromatic illumination at a wavelength λ on the front surface, the generation rate of carriers at a distance x from the surface is described by

$$G(\lambda,x) = \alpha(\lambda)F(\lambda)\left[1-R(\lambda)\right]\exp\left[-\alpha(\lambda)x\right] \tag{1}$$

where $\alpha(\lambda)$ is the absorption coefficient, $F(\lambda)$ the number of incident photons per cm^2 per sec per unit bandwidth and $R(\lambda)$ is the wavelength dependent reflection coefficient. If low-injection conditions are maintained, the following one dimensional steady-state continuity equations will hold

$$G_n - \frac{n_p - n_{po}}{\tau_n} + \frac{1}{q}\frac{dJ_n}{dx} = 0 \tag{2}$$

for electrons in p-type material and

$$G_p - \frac{p_n - p_{no}}{\tau_p} - \frac{1}{q}\frac{dJ_p}{dx} = 0 \tag{3}$$

for holes in n-type material (14). Hole and electron currents will be determined by the diffusion potentials and electric fields in the semiconductor. The resulting current density equations are (14)

$$J_n = q\mu_n n_p E + qD_n\frac{dn_p}{dx} \tag{4}$$

$$J_p = q\mu_p p_n E - qD_p\frac{dp_n}{dx} . \tag{5}$$

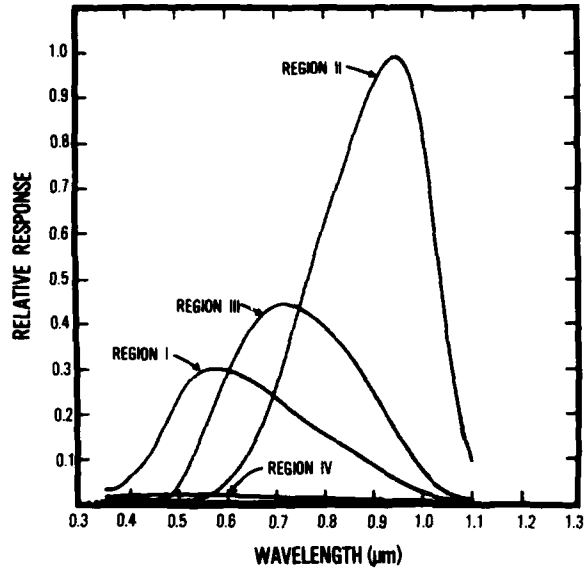


Figure 3.7. Simulation results for 11PD18M photodiode.

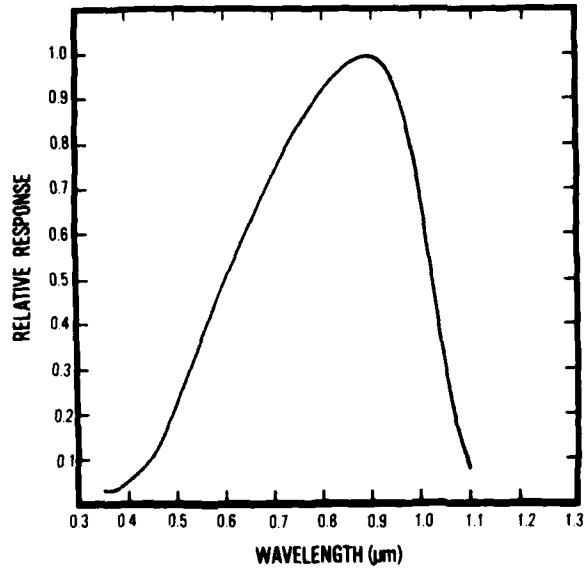


Figure 3.8. Total spectral response of 11PD18M photodiode.

TABLE 2

PARAMETER VALUES USED IN SIMULATIONS.

Structure	Region	Diffusion Coefficient $(\frac{cm^2}{sec})$	Diffusion Length (μm)	Junction Depth (μm)	Depletion Region Width (μm)
11PD18M Photodiode	p-diffusion	15	100	3.50	1.00
	n-substrate	14	125		3.25
Structure 1	n+-contact	9	37	2.84	0.58
	p-well	32	170		1.42
Structure 2	p+-contact	15	100	2.43	1.12
	n-substrate	14	125		3.38
Structure 3	p-well	32	170	6.75	1.75
	n-substrate	14	125		1.42

is due to the fact that the well depletion region that lies below the junction prohibits the diffusion of carriers back to the contact junction. Structure 2 shows a strong response from region III along with a strong response from region II. There is some response from region IV due to the fairly small area of the photodiode, which increases the relative amount of current collected by the sidewall depletion region. The response of structure 3 is similar to that of structure 2, owing to the fact that they are physically similar, structure 3 having a slightly larger active area and deeper junction depth.

Figure 3.12 compares the total responses for the three structures, assuming each structure is illuminated with the same incident light power. This would correspond to a light intensity per unit area that increases as the active photodiode area decreases ($I \times A$ = constant, where I is the incoming light intensity per unit area and A the active photodiode area). From comparison of the total responses, several conclusions can be drawn concerning the effect of physical parameters on spectral response. First, it is noted that decreasing active area and junction depth tends to flatten the spectral response and shifts the peak spectral response slightly towards shorter wavelengths. Second, the presence of a diffusion barrier below the collecting junction prevents the collection of carriers generated deep in the semiconductor and thus shifts the peak response far to the left (shorter wavelengths). Overall collection efficiency is lower, resulting in a decrease in response compared to structures with no barriers.

and proportional graphics capabilities are supported. The data of Jellison and Modine (51) was used with a cubic splines program to determine a set of polynomial functions describing the wavelength-dependent absorption and reflection coefficients. Geometrical data concerning the active area and junction depth was obtained from the previous measurements made on a 4007 integrated circuit and from data provided by the manufacturer of the sample photodiodes (52). The depletion region width on each side of the junction was obtained from Warner-Laffer curves for diffused junctions, with the reverse bias potential assumed to be six volts (53). The values used for the diffusion coefficients and minority carrier diffusion lengths were estimated from values given for various solar cell materials as detailed by Hovel (54). The final values used in the simulations are shown in Table 2. The values used for the surface recombination velocities (S_p and S_n) were 10^4 cm/sec for the front surface and 10^6 cm/sec for the backside contact. Numerical simulations were carried out for incoming wavelengths ranging from 0.3 to 1.1 μm and a constant input power. The results were normalized to one and plotted to show relative spectral response. Calculations of responsivity were also made and are compared to experimental values in Chapter IV.

Figure 3.7 illustrates the responses from regions I-IV, and Figure 3.8 the total response for a commercial photodiode having an effective area of 9.5×10^5 μm^2 and an approximate junction depth of 3.5μm. The majority of the photocurrent comes from region II, and gives the photodiode a peak spectral response at 0.9μm. Region IV does not contribute significantly to the total photocurrent, primarily due to the fact that the active junction area in regions I and II is large compared to the vertical area of region IV.

Figures 3.9, 3.10, and 3.11 show the relative contributions of regions I-IV for structures 1, 2, and 3 respectively. It is observed that for structure 1 the contribution from region II is not as predominant as for the other structures. This

$$J_{II}=\frac{qF(1-R)\alpha L_n}{(\alpha^2 L_n{}^2-1)}$$

$$x\left[\frac{\exp(-\alpha x_p)}{C}\left(\coth\frac{H}{L_n}-\tanh^2\frac{x_p}{L_n}\coth\frac{T}{L_n}-C\tanh\frac{x_p}{L_n}-C\alpha L_n\right)\right.$$

$$\left.+\frac{\exp(-\alpha H)}{C\sinh\frac{T}{L_n}}\left(\tanh\frac{x_p}{L_n}\sinh\frac{x_p}{L_n}-\cosh\frac{x_p}{L_n}\right)\right] \qquad (25)$$

where

$$C=(1-\tanh\frac{x_p}{L_n}\coth\frac{H}{L_n})$$

The total current contribution from region II is obtained by multiplying Equation 25 by the area A_{II}. The total photocurrent is the sum of the current contributions of regions I-IV.

3.2.4 SPECTRAL RESPONSE SIMULATIONS.

Having solved the necessary equations to describe the generation of photocurrent in p-n structures, it was possible to perform numerical simulations for various structures to understand the photocurrent contributions from different regions of the device and predict the total spectral response. To perform the simulations, the equations developed in Sections 3.2.2 and 3.2.3 were implemented on a Tektronix 3260 Automated Microcircuit Tester running a Tektronix operating system. While this system is primarily intended for electrical testing of microcircuits, it is also suitable for numerical simulations, as a Fortran-like language

excess carrier density is reduced to zero by the electric field in the depletion region, we can apply the same boundary condition at the edge of the well depletion edge as is applied at the diffused junction depletion edge. Specifically,

$$(n_p - n_{po}) = 0 \qquad \text{at } x_n \text{ (where } x_n = x_j + W_n) \tag{21}$$

$$\text{and } (n_p - n_{po}) = 0 \qquad \text{at H} \tag{22}$$

where H is the distance from the surface to the edge of the well depletion region. By applying these boundary conditions to

$$(n_p - n_{po}) = A\cosh\left(\frac{x}{L_n}\right) + B\sinh\left(\frac{x}{L_n}\right) - \frac{F(1-R)\tau_n}{(\alpha^2 L_n^2 - 1)} \exp(-\alpha x) \tag{23}$$

the constants A and B can be obtained.

Determination of the constants and application of

$$J_n = qD_n \frac{dn_p}{dx} \tag{24}$$

yields the solution

where W is the total depletion region width. Equation 18 can then be integrated to find the total current contribution from region IV. Integration from $x=x_p$ to $x=0$ yields

$$I_{IV}=PWqF(1-R)\left[1-\exp(-\alpha x_p)\right] \tag{19}$$

where P is the perimeter of the vertical depletion region edge.

The total photocurrent at a given wavelength is the sum of Equations 12, 16, 17, and 19:

$$I_{ph}(\lambda)=I_I(\lambda)+I_{II}(\lambda)+I_{III}(\lambda)+I_{IV}(\lambda). \tag{20}$$

3.2.3 SOLUTION FOR WELL DEPLETION EDGE BOUNDARY CONDITION.

By examination of the structure illustrated in Figure 3.5, it is clear that the solutions for the current contributions from regions I, III and IV will be the same as for the previous structure discussed in Section 3.2.2, once the appropriate changes in subscripts are made. Thus for region I we can substitute S_p, L_p, D_p and x_p for S_n, L_n, D_n and x_n in Equation 12 to obtain the current contribution. In a similar fashion, substitution of x_p for x_n and x_n for x_p in Equations 17 and 19 will yield the wavelength dependent solutions from regions III and IV.

The solution for region II is not as simple to obtain since the former boundary condition, that surface recombination takes place at the backside contact, is no longer applicable. The fact that there is a depletion region that exists between the collecting junction we are modeling and the wafer backside will prevent the diffusion of carriers from deep in the semiconductor to the junction. Since the

The total hole current collected at the junction edge with area A_{II} is

$$I_{II} = \left[\frac{A_{II} qF(1-R)\alpha L_p}{(\alpha^2 L_p^2 - 1)} \exp(-\alpha x_n)\right] \quad x$$

$$\left[\alpha L_p - \frac{\left(\frac{S_p L_p}{D_p}\right)\left(\cosh\frac{T'}{L_p} - \exp(-\alpha T')\right) + \sinh\frac{T'}{L_p} + \alpha L_p \exp(-\alpha T')}{\frac{S_p L_p}{D_p}\sinh\frac{T'}{L_p} + \cosh\frac{T'}{L_p}}\right] \tag{16}$$

In region III it is assumed that all of the generated minority carriers are swept across the junction before they can recombine, and thus contribute to the current. The current is thus equal to the number of photons absorbed which can be found by integration to be

$$I_{III} = A_{III} qF(1-R)\left[\exp(-\alpha x_p) - \exp(-\alpha x_n)\right] \tag{17}$$

where A_{III} is equal to the surface area of region III.

The current contribution from region IV is also assumed to be due to the carriers generated within the depletion region but it is seen that the vertical junction produces a depth-dependent current density

$$J_{IV}(x) = W\ \alpha F(1-R)\exp(-\alpha x) \tag{18}$$

To obtain the current contribution from region II, Equations 1, 3, and 5 are used with the boundary conditions

$$p_n - p_{no} = 0 \qquad \text{at } x = x_n \tag{13}$$

$$D_p \frac{dp_n}{dx} = S_p (p_n - p_{no}) \qquad \text{at } x = T \tag{14}$$

where x_n is the distance from the surface to the depletion region edge in the substrate ($x_n = x_j + W_n$) and T is the distance from the surface to the backside contact. The hole distribution in the substrate is found to be

$$(p_n - p_{no}) = \left[\frac{\alpha F (1-R) T_p}{(\alpha^2 L_p^{\,2} - 1)} \exp(-\alpha x_n)\right] \times$$

$$\left[\frac{\left(\frac{S_p L_p}{D_p}\right)\left[\cosh\frac{T'}{L_p} - \exp(-\alpha T')\right] + \sinh\frac{T'}{L_p} + \alpha L_p \exp(-\alpha T')}{\frac{S_p L_p}{D_p}\sinh\frac{T'}{L_p} + \cosh\frac{T'}{L_p}} \sinh\frac{x-x_n}{L_p}\right.$$

$$\left. - \cosh\frac{x-x_n}{L_p} + \exp\left[-\alpha(x-x_n)\right]\right] \tag{15}$$

where $T' = T - x_n$.

and at the depletion edge the excess carrier density is small due to the electric field in the depletion region and $n_p - n_{po} = 0$ at $x = x_p$. The resulting electron density in the p-region is

$$n_p - n_{po} = \left[\frac{\alpha F(1-R)\, T_p L_n}{(\alpha^2 L_n^2 - 1)}\right] \times$$

$$\left[\exp(-\alpha x) + \frac{\left(\frac{S_n L_n}{D_n} + \alpha L_n\right) \sinh \frac{x_p - x}{L_n} + \exp(-\alpha x_p) \frac{S_n L_n}{D_n}\left(\sinh \frac{x}{L_n} + \cosh \frac{x}{L_n}\right)}{\frac{S_n L_n}{D_n} \sinh \frac{x_p}{L_n} + \cosh \frac{x_p}{L_n}}\right]. \tag{10}$$

Since electric fields outside the depletion region are considered to be zero, Equation 4 reduces to

$$J_n = qD_n \frac{dn_p}{dx} \tag{11}$$

The current contribution from region I is found by evaluating Equation 11 at the depletion region edge x_p and multiplying by A_p the area of region I. The resulting electron current contribution is

$$I_I = \left[\frac{A_I q F(1-R)\, \alpha L_n}{(\alpha^2 L_n^2 - 1)}\right] x$$

$$\left[\frac{\left(\frac{S_n L_n}{D_n} + \alpha L_n\right) - \exp(-\alpha x_p)\left(\frac{S_n L_n}{D_n} \cosh \frac{x_p}{L_n} + \sinh \frac{x_p}{L_n}\right)}{\frac{S_n L_n}{D_n} \sinh \frac{x_p}{L_n} + \cosh \frac{x_p}{L_n}} - \alpha L_n \exp(-\alpha x_p)\right]. \tag{12}$$

For the solutions in all regions the following assumptions are made:

1. All minority carriers which reach the depletion region edge are swept across the junction.
2. No electric fields exist outside the depletion region.
3. The lifetime, mobility, and doping are constant throughout the diffused region and throughout the substrate or p-well.
4. Low-injection conditions are maintained.
5. Lateral diffusion of minority carriers generates negligible current and can be ignored; diffusion only takes place in the x direction, where x=0 is defined as the surface and x=T is the backside contact.

3.2.2 SOLUTION FOR WAFER BACKSIDE CONTACT BOUNDARY CONDITION.

For the p-diffused region in a n-substrate Equations 2 and 4 can be combined to yield

$$D_n \frac{d^2 n}{dx^2} + \alpha F(1-R)\exp(-\alpha x) - \frac{n_p - n_{po}}{\tau_n} = 0 \qquad (6)$$

which has the general solution

$$n_p - n_{po} = A\cosh\left(\frac{x}{L_n}\right) + B\sinh\left(\frac{x}{L_n}\right) + \frac{\alpha F(1-R)\tau_n}{\alpha^2 L_n^2 - 1}\exp(-\alpha x) \qquad (7)$$

where L_n represents the diffusion length; $L_n = (D_n \tau_n)^{1/2}$. Region I has two boundary conditions, where at the surface, recombination takes place with velocity S_p and

$$D_n \frac{d(n_p - n_{po})}{dx} = -S_n(n_p - n_{po}) \quad \text{at} \quad x = 0 \qquad (8)$$

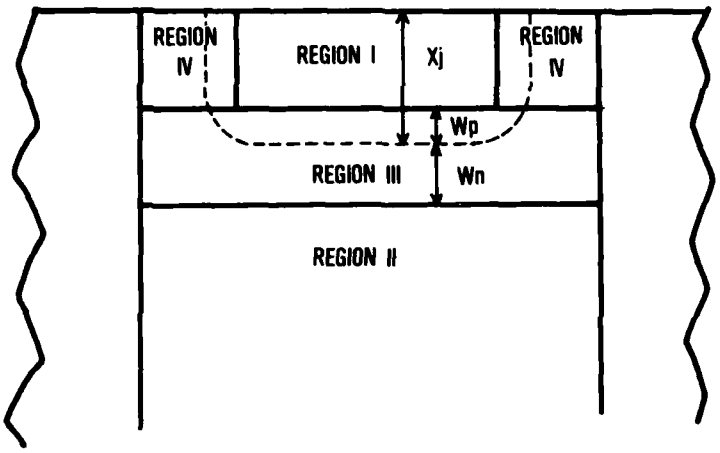


Figure 3.6. Model used to study collection of carriers.

By developing a geometrical model of the junction and applying the appropriate boundary conditions, it is possible to use equations 1-5 to find the spectral response of the junction. Time-dependent solutions can be obtained to determine the temporal response (48).

3.2 SPECTRAL RESPONSE.

3.2.1 MODELING OF CARRIER COLLECTION.

In order to accurately model carrier collection within the semiconductor, the structure was broken down into four regions, as shown in Figure 3.6. Region I is the volume within the diffused region, bounded by the surface and the three depletion edges which extend inward from the junction. Region II is the volume extending from the bottom of the depletion edge to either the backside contact or the next depletion edge, depending on the structure, and is bound on the sides by the perimeter defined by the outer depletion region edges as viewed from the surface. The bottom depletion region volume is region III, with the sidewall depletion region volume defined as region IV. Modeling of the integrated circuit structures requires two solutions, one in which region II is bounded by the wafer backside contact (describing p-diffusions into the n-substrate) and one in which region II is bounded by the p-well depletion edge (describing n-diffusions into the p-well). Solutions have been obtained for regions I and III, and for region II in the case of a wafer backside contact boundary. Hovel (49) and Sze (50) both give derivations for contributions from these regions and the solutions are repeated here, in slightly different form, for completeness. What is novel in this work is the inclusion of the current contribution from region IV, which will obviously become more important as the active area of the diode decreases, and the solution of region II when bounded by the well depletion edge.

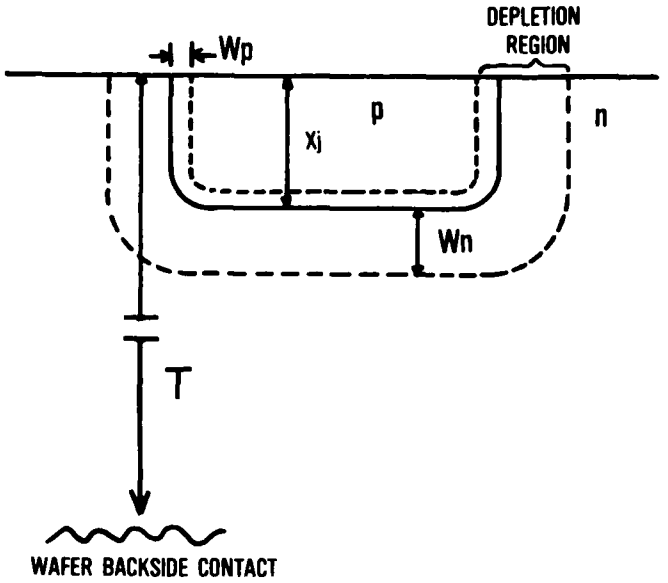


Figure 3.4. Cross section of p^+-contact to n-substrate diode structure.

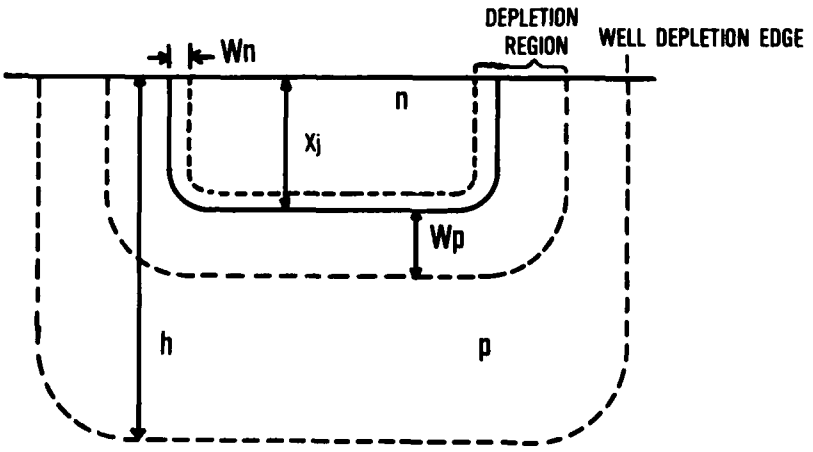


Figure 3.5. Cross section of n^+-contact to p-well diode structure.

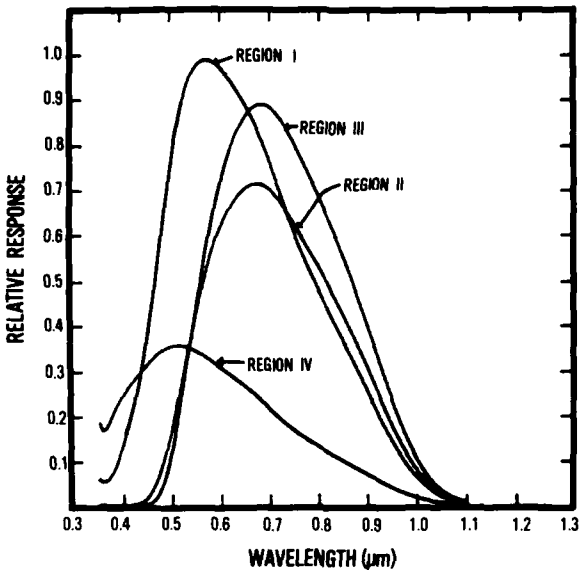


Figure 3.9. Simulation results for structure 1.

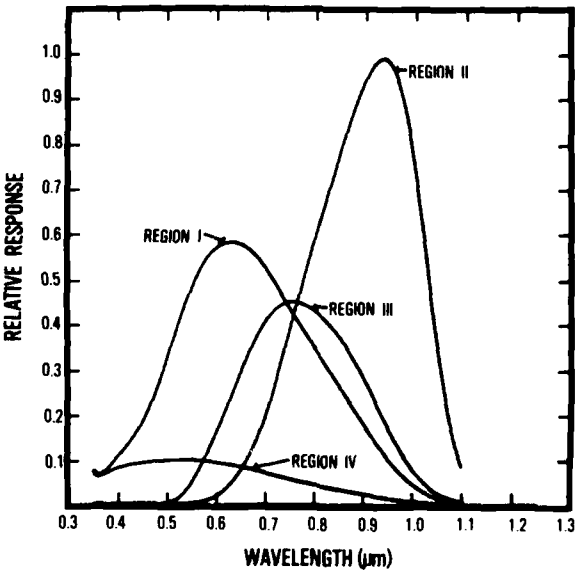


Figure 3.10. Simulation results for structure 2.

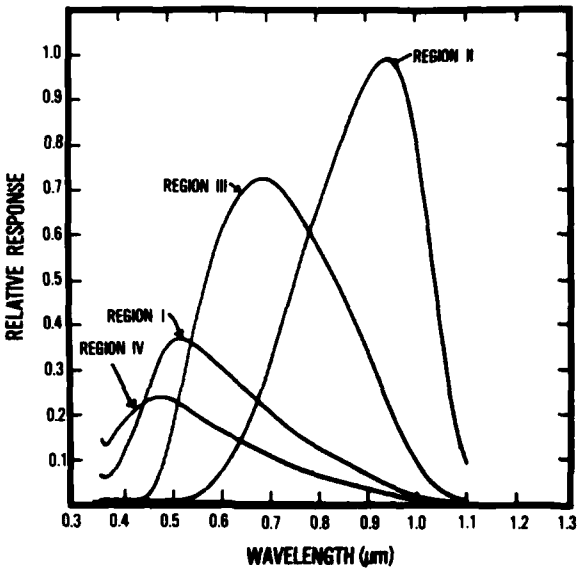


Figure 3.11. Simulation results for structure 3.

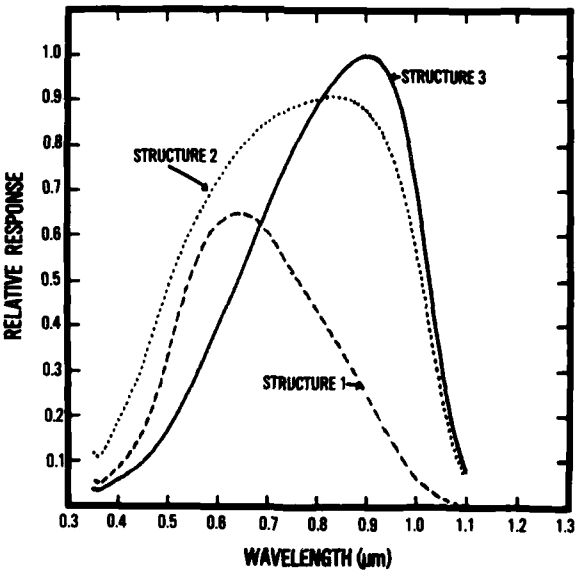


Figure 3.12. Total spectral responses for structures 1-3.

3.3 TEMPORAL RESPONSE.

To obtain the time-dependent photocurrent response of a p-n junction requires solution of the time-dependent minority carrier concentration equations. While solution of these complex equations is possible, the final time-dependent response is dependent both on the wavelength of the incoming light and on external elements (capacitance and resistance) in the circuit. Since the wavelength and circuit configuration are both application dependent it is reasonable to perform only a preliminary analysis of the temporal response, leaving solution of the time-dependent equations for specific applications analysis. Experimental work was performed to compare the temporal response of the p-n structures in the integrated circuit to that of the commercial photodiodes at 0.6328 μm. The results of this work are presented in Chapter IV.

Temporal response in non-avalanching photodiodes is dependent on three processes: charge collection time in the depletion region, diffusion time of minority carriers, and RC effects due to junction and load capacitance and resistance. Charge collection time is the time needed for carriers generated in the depletion region to be swept across the junction. For a junction depletion region that is 1.5 μm wide on one side of the junction and a saturation velocity of 10^7 cm/sec the maximum charge collection time is 15 ps, and thus would limit the maximum modulation frequency to approximately 60 GHz.

The diffusion time component of the photodiode response is strongly dependent on the wavelength of light generating the carriers. If carriers are generated deep in the substrate, the time needed for the carriers to diffuse to the depletion region edge will be large compared to the charge collection time. An approximate equation to describe the diffusion time component given in the manufacturer's literature (55) is

$$T_d = \frac{1}{13}\left[\frac{2.3}{\alpha} - 5.4\times10^{-5}(\rho V)^{1/2}\right]^2 \qquad (26)$$

where

T_d = diffusion time (sec)

α = wavelength dependent absorption coefficient (cm^{-1})

ρ = substrate resistivity (ohm-cm)

V = reverse bias voltage across the junction (volts)

Table 3 illustrates the diffusion time component for several wavelengths and absorption coefficients, assuming a resistivity of 5 ohm-cm and an external reverse bias of six volts. The rapid increase in the diffusion time component with increasing wavelength severely limits the AC response of Si photodiodes in regions above 0.7 μm.

The RC component of the rise time will depend on the capacitance and resistance in the photodiode circuit. This will vary depending on the application, and it is sufficient to note that the circuit configuration may limit the response time more than the diffusion or charge collection effects.

Figure 3.13 illustrates the simplified equivalent circuit for a photodiode. This model can be used to determine the temporal response of photodiode structures. Diffusion and charge collection effects can be modeled in the current source, along with a time-dependent description of the modulation source.

The following observations can be made concerning the temporal response of the photodiode structures in the integrated circuit.

1. Response time of the structure will depend strongly on the intensity and wavelength of the modulating source, along with the circuit load and capacitance.

TABLE 3

CALCULATED DIFFUSION TIME COMPONENTS FOR

A p-n PHOTODIODE

$\lambda(\mu m)$	(1/cm)	T_d(ns)
.422	$5.5x1^4$	4.47
.633	$3.4x10^3$	11.9
.800	$1.0x10^3$	313
.900	$5.0x10^2$	$1.4x10^3$
1.000	$1.0x10^2$	$4.0x10^4$

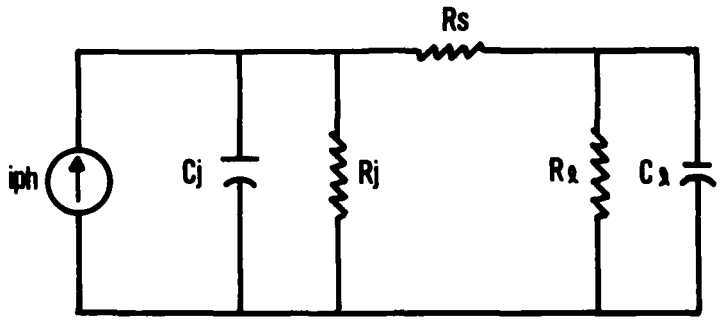


Figure 3.13. Equivalent electrical circuit for a photodiode.

2. The exact limiting mechanism (i.e., diffusion, charge collection, or capacitance) will also depend on the wavelength of the modulating source and circuit load and capacitance.

3. Performance of the integrated circuit photodiode structures should be equivalent at some wavelengths to that of the commercial p-n structures, as the structure is similar. Thus, if optimized by circuit configuration and choice of wavelength, the p-n structures in the integrated circuit should exhibit maximum modulation frequencies in the high MHz to low GHz region.

Structures 4 and 5 are phototransistor or photodiode-transistor configurations whose temporal response depends not only on the reverse biased light-collecting junction but on the additional transistor storage, rise and fall times. These times are in turn dependent on the biasing conditions and circuit configuration of the transistor. Several methods can be used to determine the temporal response and include equivalent circuit, charge control, and diffusion equation analysis (56). These structures will exhibit slower responses than those of the photodiodes due to the extra charge storage and delay introduced by the bipolar transistor. Experimental measurements of the response times were made at 0.6328μm and are presented in Chapter IV.

IV. EXPERIMENTS AND RESULTS

4.1 SPECTRAL RESPONSE.

The spectral responses of the integrated circuit structures were measured to provide experimental data to determine the accuracy of the models developed in Chapter III and also to provide experimental data to determine the usefulness of integrated detectors in different applications.

4.1.1 EXPERIMENTAL SETUP.

The spectral responses of the integrated circuit structures were determined by reverse biasing the structures in the photoconductive mode and illuminating them with a variable wavelength monochromatic source while measuring the current produced. The setup used is illustrated in Figure 4.1 and consisted of a high intensity tungsten lamp, a monochrometer and filters, a microscope, a digital electrometer and a 6V battery. Two gratings were used in the monochrometer, one in the range of 0.35 μm to 0.7 μm and another from 0.70 μm to 1.1 μm. Information provided by the manufacturer indicated that the bandwidth of the monochrometer system was approximately 13 nm in the 0.35 μm to 0.70 μm range and 26 nm in the 0.70 μm to 1.1 μm range (57). Several combinations of filters were used throughout the spectrum to filter out unwanted second-order diffraction lines. The microscope served to condense the light and by focussing with white light prior to the experiment allowed a constant working distance to be maintained. A 5X final objective was used and provided illumination of the entire sample. The electrometer was used in the current measuring mode and was suitable for measurements down to the picoampere range.

To calibrate the light source, two of the sample photodiodes were used as references. The characteristics of the 11PS18M and 22BH18M photodiodes were given in the manufacturer's literature and are illustrated in Figure 4.2. By digitizing this data and using a cubic splines program it was possible to determine a

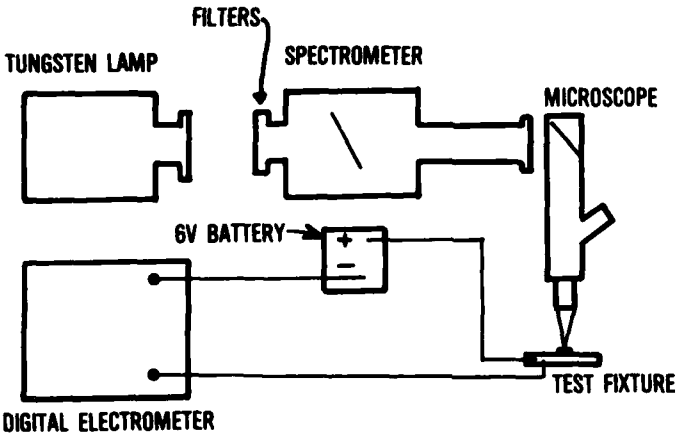


Figure 4.1. Schematic diagram of the spectral response measurement setup.

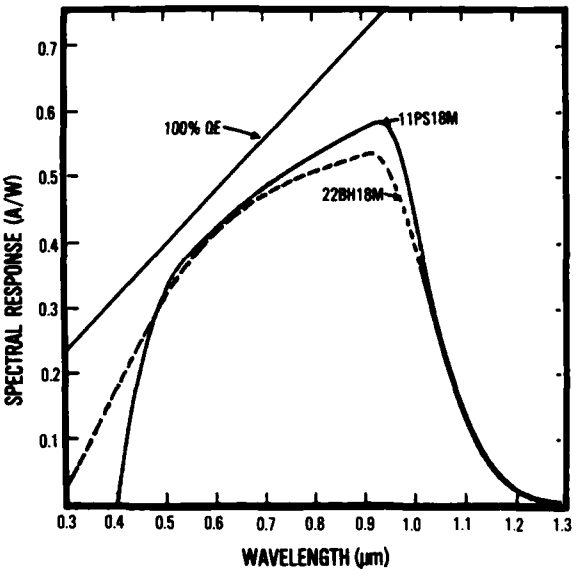


Figure 4.2. Spectral response of the photodiode samples.

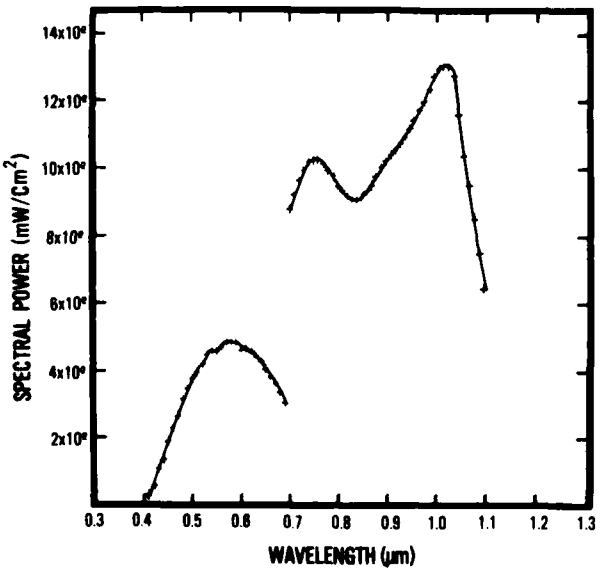


Figure 4.3. System calibration curve.

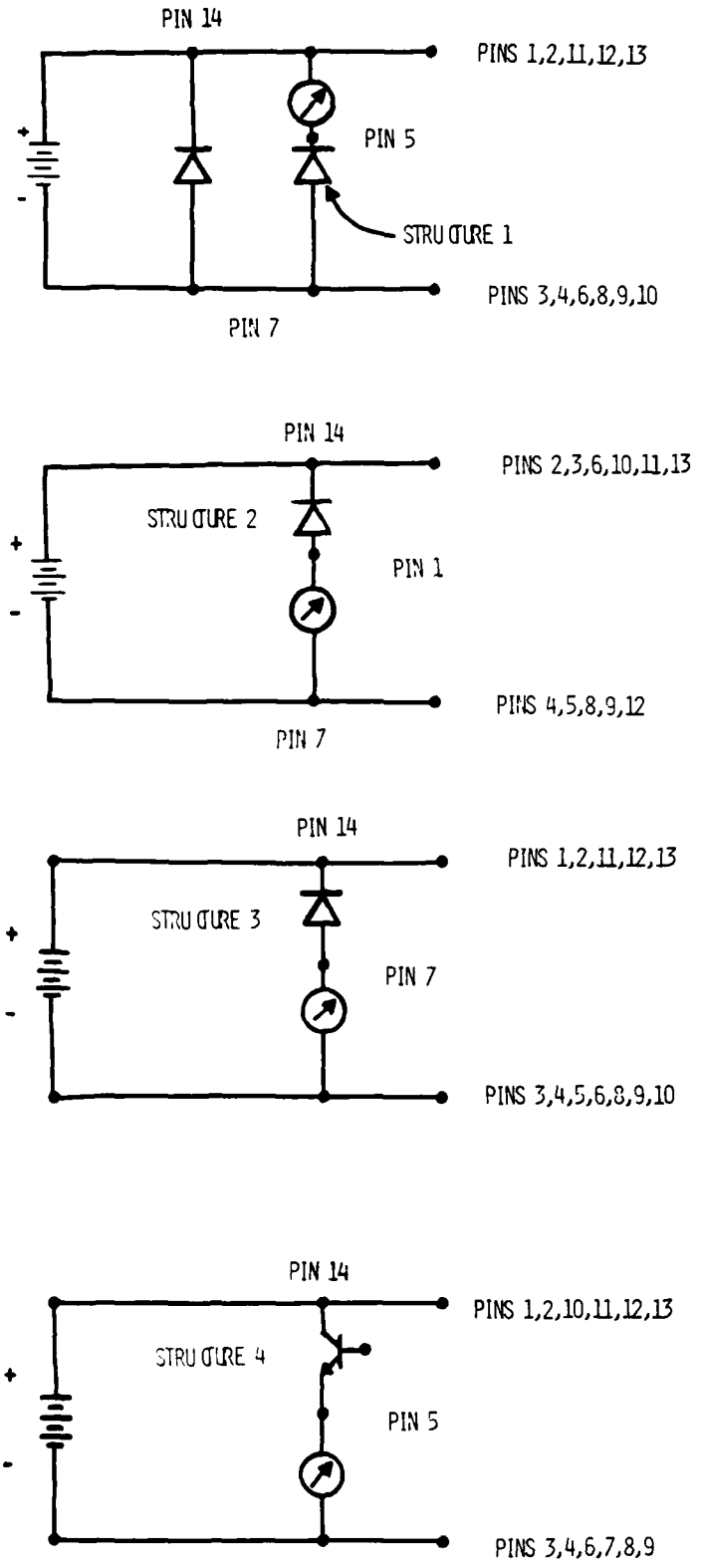


Figure 4.4. Biasing configurations used for spectral response measurements.

set of polynomial functions which described the spectral response of the photodiodes. Using the experimental setup, the reverse biased diodes were then illuminated with monochromatic light from 0.35μm to 1.1μm in increments of 0.01μm with the current produced at each step recorded. By dividing the current produced by the given responsivity in A/W, the total light input power was obtained. Further division by the active area of the photodiode produced the light power per unit area as a function of wavelength. Two sets of data from the 22BH18M photodiode and one set from the 11PS18M photodiode were taken and averaged to obtain the system calibration curve illustrated in Figure 4.3. The discontinuity seen at 0.7μm is due to the fact that two separate gratings had to be used, the one in the 0.7 to 1.1μm range having a much higher throughput. It was noted that the power curve for the system does have the characteristic shape that would be expected for a hot black body source such as a tungsten lamp, with the falloff in the 1.1μm range due to the low transmission of the microscope optics in the infrared range.

Spectral response measurements were made on the 11PD18M photodiode and on structures in three integrated circuit samples. Sample 1 was a 4007 on which the glass passivation layer was thinned by etching with a commercial glass etch (Siloxide) for four and one-half minutes. The remaining passivation layer was estimated to be several hundred nanometers thick. Measurements were made on structures 1-4 of sample 1 with the structure of interest reverse biased and all other pins floating. Samples 2 and 3 were 4007's which received no special preparation. Spectral responses for structures 1-4 on samples 2 and 3 were measured with the structure of interest reverse biased and the remaining pins biased in a configuration in which the other junctions in the integrated circuit were shorted and thus did not generate any circuit photocurrent. The biasing configurations used are illustrated in Figure 4.4. For each structure, three sets of data were

taken from each sample. Dark current measurements were taken at several points during the spectral response measurements and the average dark current measurement was subtracted from the data. The three sets of data taken on each structure were then averaged and normalized to unity to produce the final spectral response.

4.1.2 RESULTS.

The results of the spectral response measurements are illustrated in Figures 4.5-4.13 and are compared with the simulated spectral responses, except for structure 4 which is a phototransistor structure which was not simulated. The parameters used in the simulations were identical to the ones presented in Chapter III, except for the active areas which were modified to account for the metallization which covers much of the surface. The active areas of structures 1 and 2 were multiplied by 0.3 and the active area of structure 3 multiplied by 0.6. This decreased the response of regions I, II and III relative to the response from region IV and shifted the peak spectral response slightly towards shorter wavelengths. The spectral response for structure 5 was not measured as it was not possible to selectively illuminate the photodiode in the structure.

Figure 4.5 illustrates the spectral response for the 11PD18M photodiode, which was the sample photodiode not used to calibrate the system. The measured spectral response is close to that predicted by theory, with a peak at 0.9μm. These results indicate a fairly good correlation between the theoretical and experimental work and also are supported by the manufacturer's data on the photodiode. The spectral response for structure 1 is illustrated in Figures 4.6 and 4.7 and is compared to the theoretical response. Again there is good correlation between the experimental values and the theoretical prediction, with the exception of an anomalous peak seen near 0.42μm and a discontinuity at 0.7μm. The spectral responses for structures 2 and 3 indicate a peak spectral response at a much shorter wavelength than predicted. Structure 4 indicates a response similar

› that of structure 3. This is as expected, since it is the same junction which enerates the photocurrent and is only amplified by vertical transistor action in tructure 4.

The peak near 0.42μm is observed in the spectral responses of all the tructures in the integrated circuit, along with the discontinuity at 0.7μm. The iscontinuity is due to the fact that the grating in the monochrometer had to be hanged at 0.7μm during the measurement of each structure. Any slight ıovement of the monochrometer caused a change in the light intensity reaching he sample, and is seen as a discontinuity in the spectral response. The strong pectral response at 0.42μm is thought to be due to a photoluminescent effect /hich originates in the glass passivation of the device. Manufacturers of ıtegrated circuits often employ a phosphorous doped glass as a passivation layer, he main function of the phosphorous being to getter mobile surface ions (usually la ions) which may cause surface inversion problems. The phosphorous in the glass orms a series of compounds from P_2O_5 up to about $5Na_20.3P_2O_5$ (58), which are nown to have flourescent and phosphorescent properties (59). It is thought that in his case the phosphorous compounds photoluminesce and convert the incoming ight in the UV range to light in the visible to near IR range. The conversion of the ight would give the appearance of a high spectral response in the UV range. It is ossible that interferometric effects caused by the passivation produce the peak, ut the sharpness of the peak and lack of other corresponding interferometric eaks make this possibility unlikely. The appearance of the peak in both sample 1 /here the passivation has been thinned, and in samples 2 and 3 where the assivation was the original thickness confirmed that the peak was not interfero- ıetric in nature. Some interferometric effects were observed on samples 2 and 3 /hich were not as pronounced on sample 1. The biasing of the unused external pins lid not have any effect on the spectral responses of the structures.

ıult in electrical current. The quantum efficiency can be calculated from the ıponsivity:

$$QE = \frac{1.24R}{\lambda} \tag{27}$$

ıere R = photodiode responsivity in A/W and λ is the incoming wavelength in μm. ıe quantum efficiencies for the integrated circuit structures are given in Table 6, ɔng with the responsivities for structures 4 and 5. The quantum efficiencies for ructures 4 and 5 are meaningless since they employ electrical gain, but their gain ctors (betas) were calculated and found to be 73.88 and 43.59 respectively. The :ak spectral response for structure 5 was assumed to be at the same wavelength the peak response for structure 1, since structure 1 supplies the base current to ıe transistor in structure 5.

TABLE 6

MEASURED AND CALCULATED RESPONSIVITIES.

Structure	Peak Spectral Response (μm)	Responsivity at 0.6328μm (A/W)	Responsivity at Peak (A/W)	Quantum Efficiency at Peak
Structure 1	0.70	0.40	0.42	74.4%
Structure 2	0.65	0.45	0.47	89.7%
Structure 3	0.70	0.47	0.49	86.8%
Structure 4	0.70	34.53	36.35	-
Structure 5	-	17.27	18.18	-

4.3 RESPONSIVITY AND QUANTUM EFFICIENCY.

In order to determine the relationship between the light input power and the current generated in the structures, the responsivities of the integrated circuit structures were measured and the quantum efficiencies calculated. These results were compared with calculated values as determined by solution of the diffusion equations (Chapter III).

4.3.1 EXPERIMENTAL SETUP.

The laser setup previously described and illustrated in Figure 4.13 was used to determine the responsivity of the photodiodes in the spot mode at 0.6328 μm. The structures were illuminated near the junction edge where the entire beam was able to penetrate the surface, unobstructed by surface metallization. The light power reaching the surface was determined using the sample photodiodes with known responsivities and was found to be 0.695 mW. This value was used to determine the responsivity of the integrated circuit structures at 0.6328 μm. The responsivity at the experimental peak was then calculated from the responsivity at 0.6328 μm and the experimental spectral response.

4.3.2 RESULTS.

Table 6 compares the spectral response peaks and responsivities as obtained from theory and experiment. The responsivities obtained from the simulations do not take into account the effect of the passivation on the device which may serve as an antireflective coating and increase responsivity. The calculated values were also based on broad illumination whereas the measured values are for spot illumination.

Another common measure of the efficiency of a photodiode for converting light to electrical current is the quantum efficiency. A quantum efficiency of 100% indicates that all of the photoexcited minority carriers are collected and

TABLE 5

MEASURED TEMPORAL RESPONSES.

Structure	Experimental Rise Time 10-90% (ns)
11PD18M Photodiode	150
Structure 1	120
Structure 2	150
Structure 3	150
Structure 4	600
Structure 5	600

made with the structure in the photovoltaic mode with a resistive load of 50 ohms. External capacitance due to the test fixture and cables was estimated to be 30 pf.

4.2.2 RESULTS.

The rise time of the 11PD18M photodiode, as stated by the manufacturer, is 10 ns with a 50 ohm load and was determined using a GaAlAs laser with a negligible rise time. The measured rise time in this experimental setup was 150 ns, due to the rise time of the modulator and the circuit capacitance.

A comparison of the measured rise times is given in Table 5. The commercial photodiode and structures 1-3 were all observed to have similar rise times in the experimental setup. Structure 4 had a much longer rise time due to charge storage in the base region. The photodiode-transistor configuration (structure 5) was observed to have a similar rise time, again due to charge storage in the base region.

Due to the relatively long rise time of the modulator it was not possible to determine the minimum rise times for the integrated circuit structures. However, examination of the structure of the integrated circuit photodiodes indicates that their temporal response should be close to that of commercial photodiodes as they are physically similar. The rise time of structures 1-3 is thus predicted to be on the order of 10 ns and may actually be somewhat better due to the reduced junction capacitance as compared to that of the commercial photodiodes which have a much larger junction area and thus larger capacitance. The rise times of structures 4 and 5 were measured to be almost two orders of magnitude larger than the photodiode structures. This is as expected since the gain of the transistors employed in these structures range from a beta of 50-100. If the simplifying assumption is made that the rise and fall times are proportional to the gains of the transistors the minimum rise times should be on the order of 500-1000 ns.

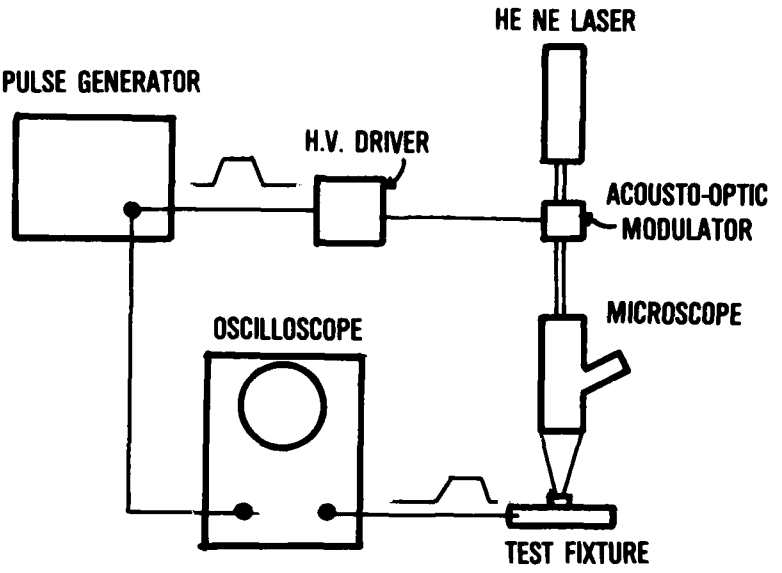


Figure 4.14. Schematic diagram of the temporal response and responsivity measurement setup.

2 and 3 (junctions formed by contacts into the substrate) are inaccurate. To accurately model structures 2 and 3 the doping profile in the substrate would need to be determined, and solutions to the diffusion equation which account for a non-zero electric field need to be solved. If the field, lifetime and mobility can be approximated to be constant throughout the diffused region, analytical solutions can be obtained. Otherwise, numerical methods can be used to obtain the spectral response (61).

4.2 TEMPORAL RESPONSE.

The temporal responses of the integrated circuit structures were measured using a HeNe laser operating at 0.6328 μm. These measurements served as the basis for comparison of the response speed of the integrated circuit structures as compared to that of the photodiodes. The experimental setup was not adequate for a direct measurement of the rise time of the photodiode structures but was sufficient for comparative measurements.

4.2.1 EXPERIMENTAL SETUP.

Figure 4.14 illustrates the experimental setup used to measure the temporal response. The setup consisted of 5 mW HeNe laser, an acousto-optic modulator, pulse generator, high voltage driver, test fixture, and oscilloscope. The laser beam was passed through the modulator so that the second order beam was aligned with the center of the optical column. The beam was focused on the surface of the device to a spot size of approximately 5 μm. A five volt signal from the pulse generator was used to modulate the high voltage driver for the acousto-optic modulator. The rise time for the pulse generator was on the order of 5 ns but the acousto-optic modulator had a much longer rise time. The laser used had a beam diameter of 0.85 mm and the rise time for the modulator as estimated from the manufacturer's literature was 100 ns (62). Measurements were made on the 11PD18M photodiode and on structures 1-5 on sample 1. The measurements were

The poor correlation between the experimental and theoretical spectral responses for structures 2 and 3 indicates some fault with the assumptions made to develop the solutions for the diffusion of carriers in the semiconductor. The assumption that the lifetime, mobility and doping density are constant on each side of the junction is a simplification. It is clear that the diffusion of dopants from the surface generates a doping profile that is not constant. For low doping densities this assumption will remain valid as the electric field created by the doping profile will have little effect on the diffusion of optically generated carriers, and the change in lifetime and mobility will be small. At higher doping densities these effects must be considered as the short wavelength response of the structure will be greatly affected. For the integrated circuit structures however, it is noted that the disagreement between experiment and theory is not as great at the shorter wavelengths as at the longer wavelengths (0.8μm). This indicates that the assumption that the mobility, doping and lifetime in the substrate is at fault.

It is known that the doping density in the substrate decreases as a function of distance from the surface. This is due to the fact that the impurities are diffused from the surface from an unlimited (gaseous) source. The dopant profile creates an electric field which opposes the diffusion of minority carriers towards the junction. This decreases the spectral response from region II and causes the overall response of the photodiode to be low in the IR region of the spectrum. It is noted that if the concentration gradient is low near the junction and increases towards the back contact the electric field created aids minority carriers in diffusing towards the junction. Solar cells are sometimes fabricated with such fields in the base region for enhanced response (60).

The presence of an electric field in the substrate of the integrated circuit could explain why the simulations of the commercial photodiode and structure 1 are fairly close to the experimental results and why the simulations for structures

TABLE 4

EXPERIMENTAL AND PREDICTED SPECTRAL RESPONSES.

Structure	Peak Spectral Response (μm) Theory	Peak Spectral Response (μm) Experiment	Responsivity at Peak (A/W) Theory	Responsivity at Peak (A/W) Experiment
UPDI8M Photodiode	0.90	0.88	0.44	0.42
Structure 1	0.64	0.70	0.27	0.42
Structure 2	0.85	0.65	0.38	0.47
Structure 3	0.90	0.70	0.42	0.49

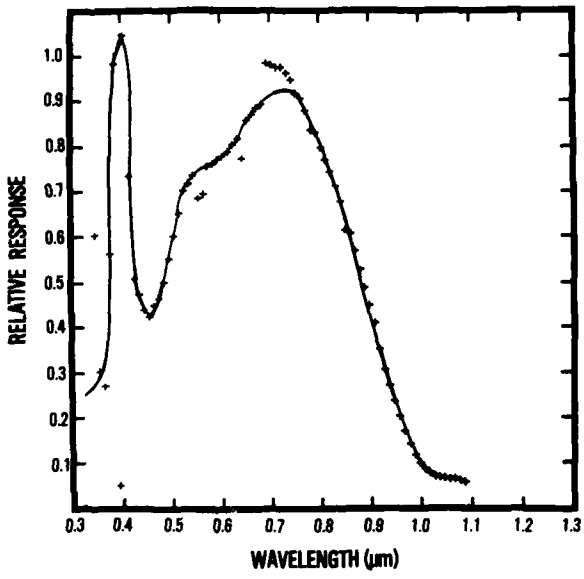


Figure 4.12. Spectral response of structure 4; sample 1.

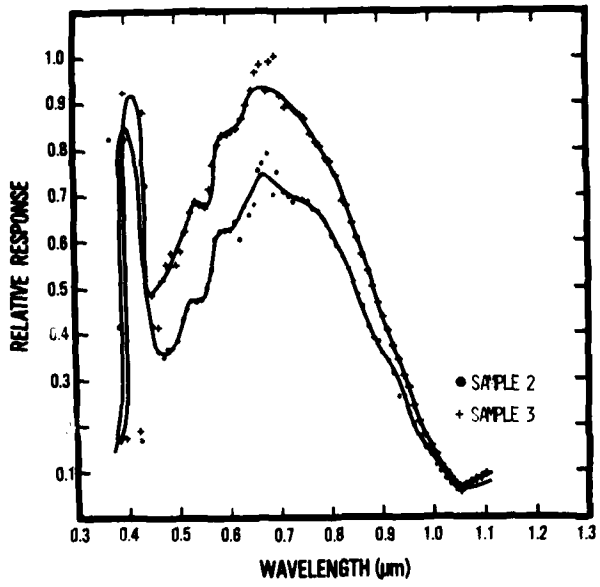


Figure 4.13. Spectral response of structure 4; samples 2,3.

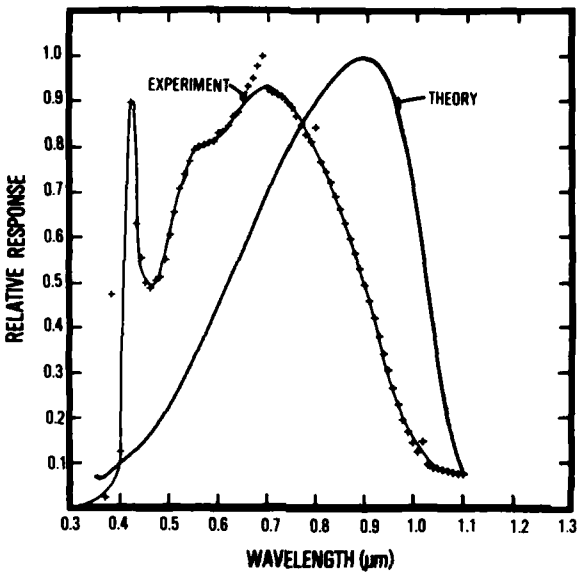


Figure 4.10. Spectral response of structure 3; sample 1.

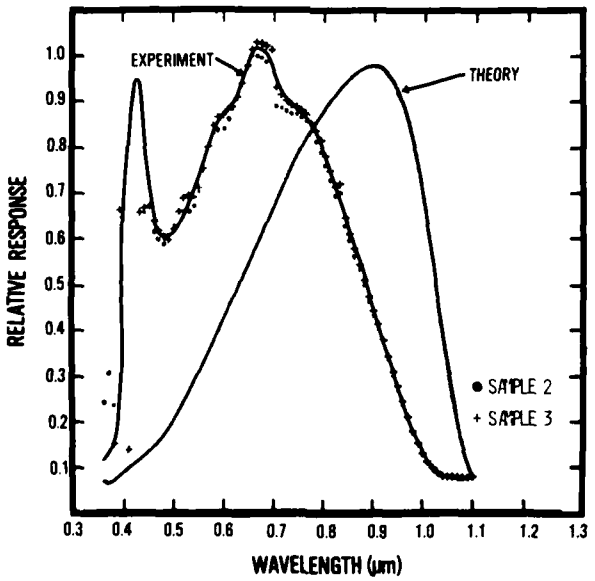


Figure 4.11. Spectral response of structure 3; samples 2, 3.

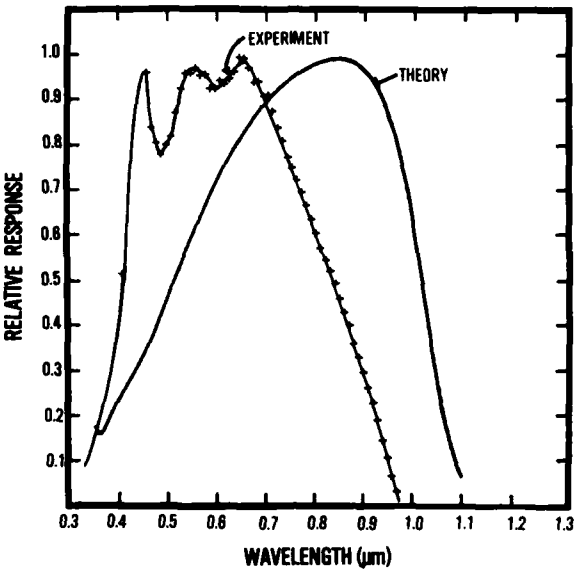


Figure 4.8. Spectral response of structure 2; sample 1.

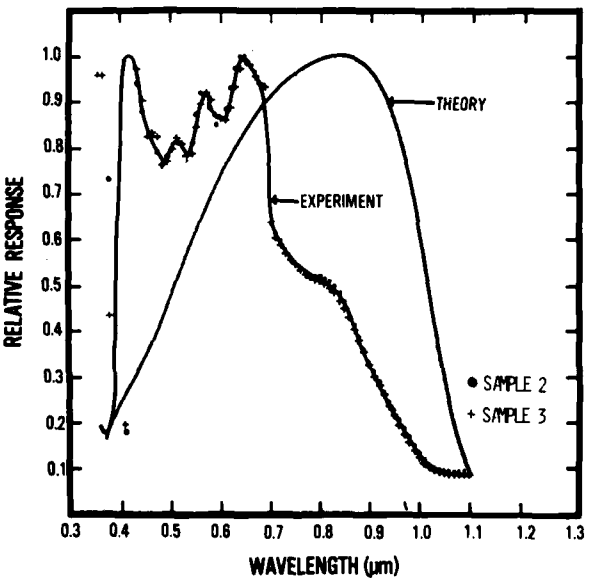


Figure 4.9. Spectral response of structure 2; samples 2,3

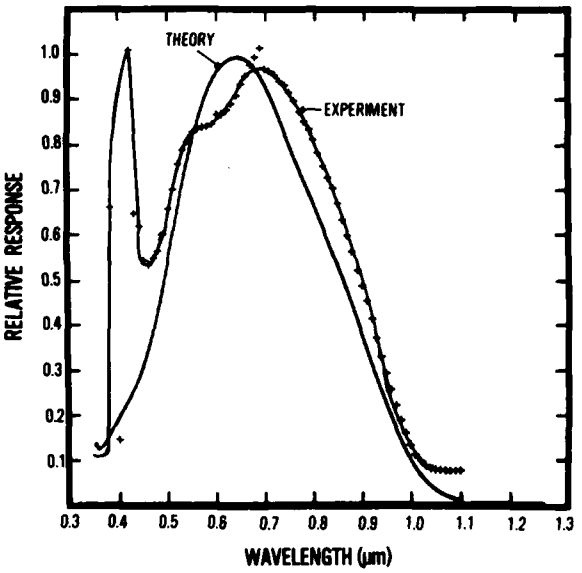


Figure 4.6. Spectral response of structure 1; sample 1.

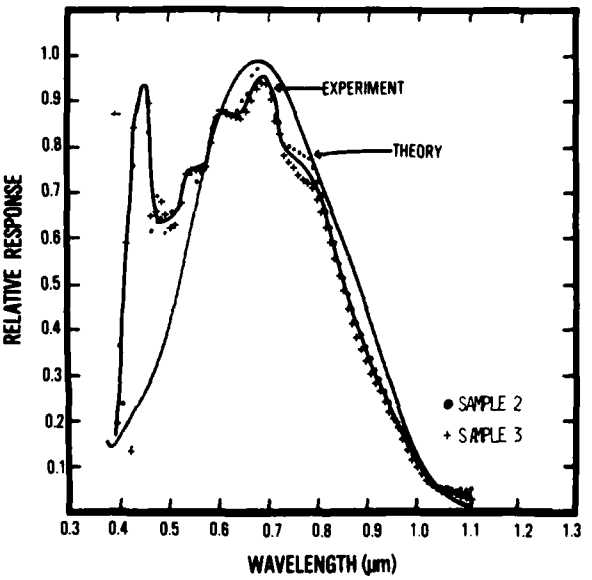


Figure 4.7. Spectral response of structure 1; samples 2, 3.

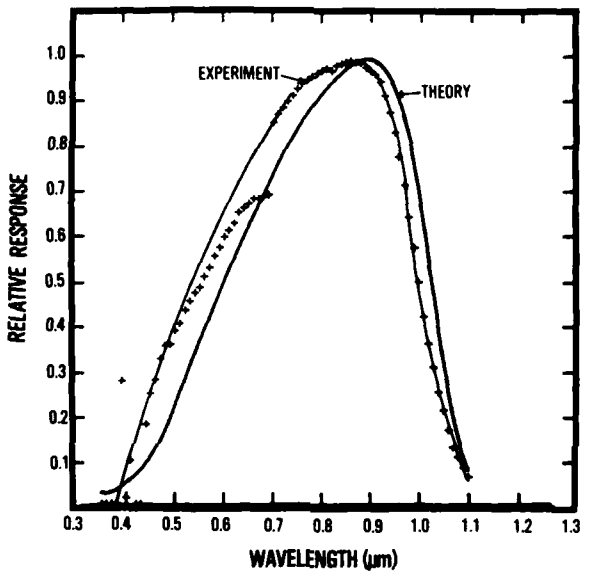


Figure 4.5. Spectral response of the 11PD18M photodiode.

V. PERFORMANCE EVALUATION.

5.1 GENERAL DISCUSSION.

In order to evaluate the use of the structures as photodetectors, the data of the preceding two chapters are summarized in this section. From this we can determine how well the structures will be able to be used in the two main applications considered, the laser testing of integrated circuits and VLSI opto-electronic devices.

The spectral response of structure 1 was predicted to decrease sharply near 1.0 μm due to the presence of the well depletion region which acts as a diffusion barrier. This was predicted correctly. The minimum rise time could not be determined experimentally but is predicted to be equivalent to that of commercial photodiodes; on the order of 10 ns or less. The measured peak responsivity for structure 1 was 0.42 A/W as compared to the calculated value of 0.27 A/W. The difference is due to both passivation effects and more importantly due to the fact that the measurements were made in the spot mode with the beam position near the vertical edge of the junction. The calculated value was for broad uniform illumination and is expected to be lower as the average response of the structure (regions I-IV) at 0.6328 is less than the response for the junction edge (predominantly region IV).

Structures 2 and 3 were expected to have similar responses to that of the commercial photodiodes but instead had responses that decreased rapidly at wavelengths above 0.90 μm. This is believed to be due to presence of an electric field caused by the doping profile in the substrate. The field works against the diffusion potential in the semiconductor and reduces the number of carriers generated in the substrate which reach the depletion region edge. This effect is of critical importance in determining the spectral response of the integrated circuit structures at wavelengths above 0.9 μm. The minimum rise times for these

structures were not determined experimentally but are again expected to be similar to those of the commercial photodiodes and on the order of 10 ns. The existing electric field may decrease the rise time due to the reduction of the diffusion time component and the resulting rise times for structures 2 and 3 may be considerably shorter than the rise time of structure 1. The peak responsivities for structures 2 and 3 were found to be 0.47 and 0.49 A/W respectively, and were slightly higher than the calculated values, again due to the difference between the spot mode and broad illumination effects.

Structure 4 has the spectral response of the reverse-biased collector-base junction (structure 3) which supplies current to the base. The spectral response of structure 5 was not measured since it was not possible to selectively illuminate the n^+-contact to the p-well junction. These structures offer the advantage of direct current gain of the photocurrent with the disadvantage that the response time is much longer than that of the photodiode structures. The additional gain results in a loss of speed for the structure due to the additional charge storage of the transistor.

5.2 INTEGRATED DETECTORS FOR LASER TESTING.

The spectral and temporal responses of the structures in the integrated circuit indicate that they can serve as adequate detectors for a modulated laser signal and be used to inject test signals in an integrated circuit. In a MOS device the conventional contact-substrate junctions such as structures 1 and 2 can be used to receive signals, or special detectors with any of the configurations of structures 1-5 can be fabricated and used with special on-chip detection circuitry.

The spectral response of the structures is suitable for laser testing, considering that the test environment will allow for the choice of a laser operating at a wavelength where the structure exhibits high responsivity. HeNe operating at 0.6328 @m has been the traditional choice and is inexpensive and well suited for

the structures in the 4007 which all exhibit peak spectral responses near 0.70 μm and responsivities of approximately 0.40 A/W. For VLSI devices with shallower junctions, the peak response can be expected to be shifted towards the blue region of the visible spectrum, and a HeCd laser operating at 0.4220 μm may be a logical choice. In either case, the spectral response of the junctions is not a limiting factor for laser testing.

The temporal response of the structures indicates that in certain circuit configurations, the maximum modulating frequency will be in the high MHz range. The use of existing junctions constrains the circuit configuration and may not allow for the optimum time response.

5.2.1 USE OF EXISTING CIRCUIT JUNCTIONS FOR TESTING.

The use of existing junctions in devices as detectors for test signals was demonstrated in 1976 by Edwards, Smith and Kemhadjian, who injected test signals into the drain-substrate junctions of the inverters of a MOS shift register using a 2 mW HeNe laser operating at 0.6328 μm (63). Later work published by Smith and Oldham discussed the amount of laser power needed to test various families of integrated circuits using a HeNe laser. They found that power levels ranged from 0.081 μW for dynamic MOS devices up to 30 mW for CMOS devices operating at a power supply voltage of 10 volts (64). The technique used is illustrated in Figure 5.1 which shows the illumination of the drain of the "off" transistor and the corresponding voltage modulation at the output. To modulate the inverter, the power supply voltage is lowered until the channel current in the on-transistor is near the magnitude of the photocurrent generated. The photocurrent is then large enough to switch the output of the inverter. Using the laser setup described in Chapter IV, modulation of a CMOS inverter was demonstrated and is illustrated in Figures 5.2-5.4. Figure 5.2 illustrates the modulation of the output by illumination of the drain of the n-channel transistor, and Figure 5.3 illustrates the output

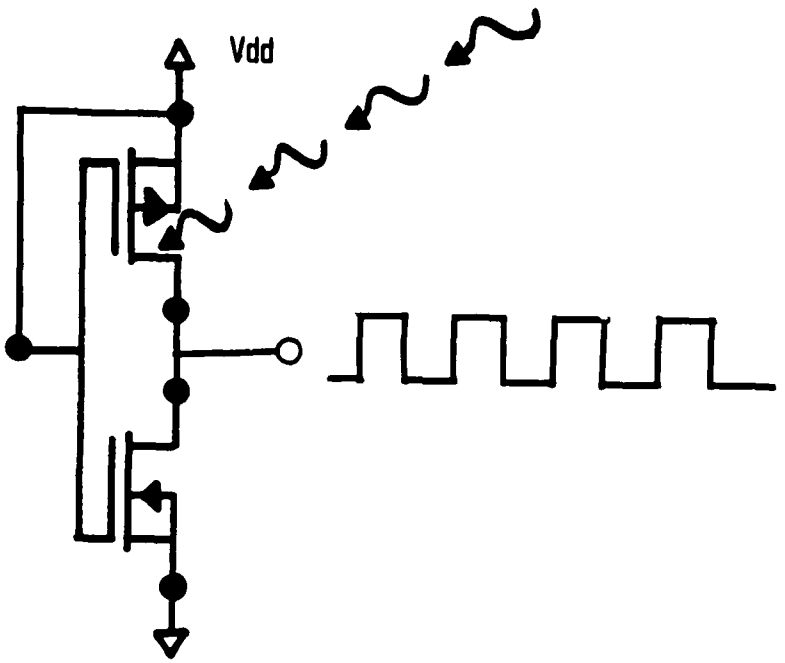


Figure 5.1. Laser signal injection on a CMOS inverter.

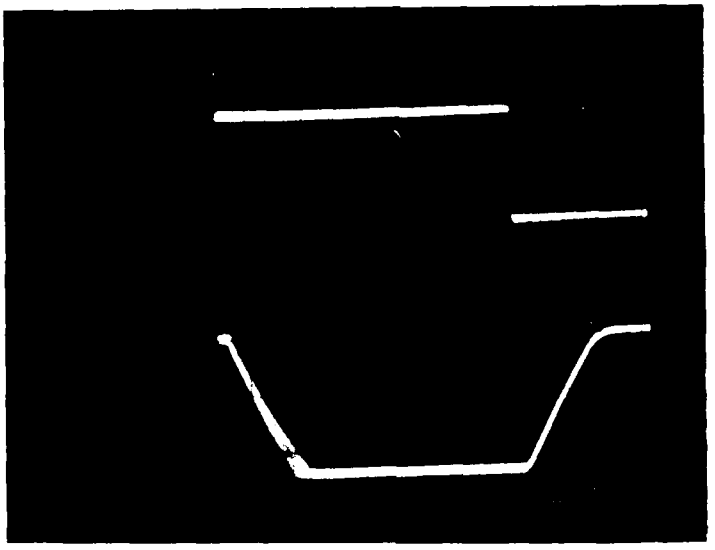


Figure 5.2. Modulation of an inverter utilizing structure 1. Upper trace is the laser modulation signal, lower trace is the inverter output. Vertical scale on upper trace is 2 volts per division, lower trace 1 volt per division. Horizontal scale is 5 @s per division. Power supply voltage was 1.90 volts.

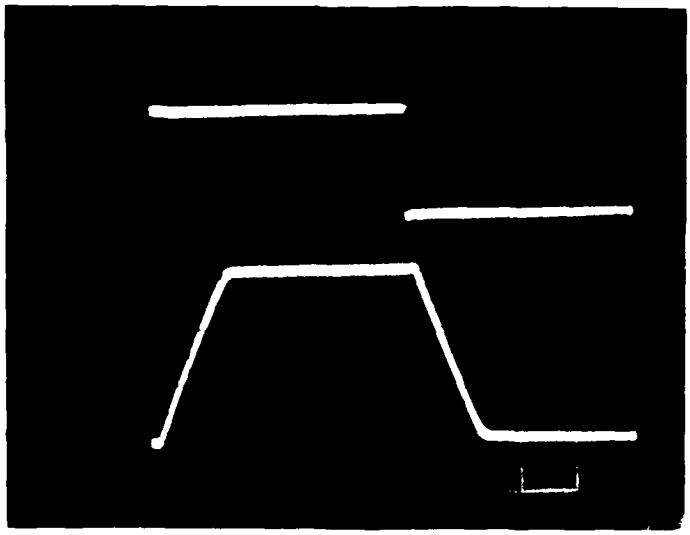


Figure 5.3. Modulation of an inverter utilizing structure 2. Upper trace is the laser modulation signal, lower trace is the inverter output. Vertical scale on upper trace is 2 volts per division, lower trace 1 volt per division. Horizontal scale is 5 μs per division. Power supply voltage was 2.5 volts.

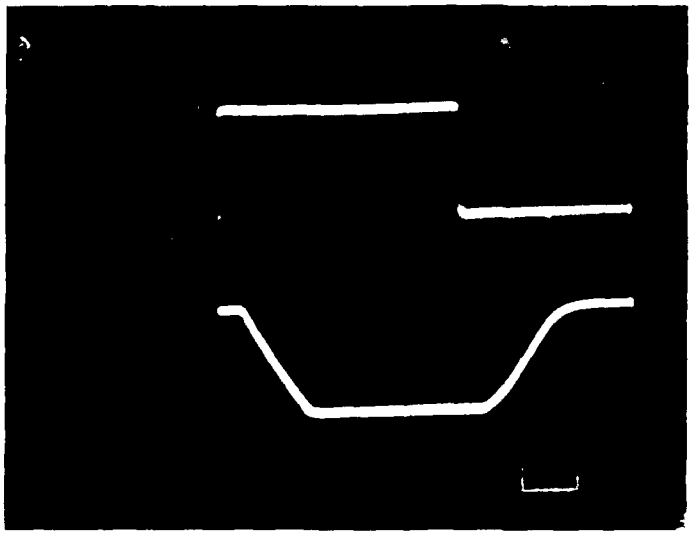


Figure 5.4. Modulation of an inverter utilizing structure 5. Upper trace is the laser modulation signal, lower trace is the inverter output. Vertical scale on upper trace is 2 volts per division, lower trace 1 volt per division. Horizontal scale is 5 μs per division. Power supply voltage was 2.23 volts.

obtained when the drain of the p-channel transistor is illuminated. If the circuit can be configured to allow the p-well to be connected separately (instead of being directly connected to the ground pin) structure 5 can be utilized to modulate the output, as illustrated in Figure 5.4.

The maximum frequency at which the circuit can be modulated is strongly dependent on the circuit configuration, transistor characteristics, laser power, and the response time of the junction. For CMOS devices the photocurrent generated by the drain-substrate junction must be at least as large as the channel current in the on-transistor in order to switch the output. The magnitude of the photocurrent with respect to the channel current, along with the sum of the capacitances at the output node, will be of primary importance in determining the response time. The time dependent solution for the output was discussed by this author in a previous publication which analyzes the effects of photocurrent on the rise and fall times of a CMOS device (65). For the laser testing of CMOS devices it will be desirable to use as powerful a laser source as possible to obtain the maximum modulation frequency. The upper limitations for the laser power will be the consideration of heating of the Si and the generation of stray carriers which may be collected by adjacent reverse-biased junctions and cause upset of the device. A simple worst-case calculation shows that for a 10 degree Centigrade difference in temperature between the surface and the backside contact of a wafer 13 mils thick, approximately 30 mW of heat energy can be conducted out of a 250 μm by 250 μm area on the backside of the wafer if the package acts as an infinite heat sink. Since only a portion of the laser energy generates heat, it is reasonable to assume that upwards of 100 mW of laser power could be safely used to generate current. In VLSI devices with highly packed transistors and geometries approaching 1.25 μm, stray currents generated by the collection of carriers at other junctions may impose a more severe restriction than heating considerations.

5.2.2 SPECIALIZED DETECTORS FOR TESTING.

The possibility of constructing specialized photodetectors for the injection of test signals in an integrated circuit offers several advantages over the use of existing junctions. First, the detection circuitry can be optimized by design for high speed response. This would allow for the injection of test signals at high frequencies, being limited only by the performance of the photodetector structure. For shallow (< 0.3 μm) p-n junctions modulated by a HeCd laser at 0.4220 μm, frequencies approaching 1 GHz should be attainable, considering that the photodiode response will be limited by charge transition times in the depletion region. Diffusion effects will be small due to the shallow penetration of the laser, and the capacitance of the junction will be small due to its small size (relative to a commercial photodiode) and shallow junction depth. A second advantage in developing integrated circuits with specialized photodetectors is that they can be designed to minimize the effects of undesired photocurrents generated while testing. A junction formed in a doped well (such as structure 1) would be ideal since the well depletion region collects laterally diffusing minority carriers and thus prevents the generation of photocurrent at other junctions.

There are several problems associated with placing specialized detectors on integrated circuits. First, the cost in silicon real estate may be prohibitive. Second, it may not be possible to develop the specialized detection circuitry needed when constrained to a digital VLSI process. Several recent advancements in the development of photoconductive circuit elements (PCE's) indicate that they may offer greater potential for use as optical test inputs than p-n structures. Eisenstadt et al. reports the development of integrated Si photoconductors with rise times of less than 2 ps (66). An article by Jain reports the use of photoconductors to determine the propagation delays of digital ICs with better than 10 ps resolution (67).

5.3 VLSI OPTOELECTRONIC DEVICES.

The development of VLSI devices employing fiber optic, waveguide or holographic elements for chip-to-chip or on-chip connections necessitates the development of on-chip detectors. Since most of the proposed interconnection schemes involve optical signals in the 0.8 μm to 13 μm range, the ability to develop p-n integrated photodetectors for this application is questionable considering their limited spectral response above 0.8 μm. Further research will be needed to confirm the presence of the electric field which limits the spectral response and to determine if it can be minimized to increase response above 0.8 μm. The intrinsic absorption characteristics for silicon will prevent its normal use as a photodetector at wavelengths above 1.1 μm although edge oriented photodetectors such as those being developed by Boyd may be used for detecting signals in the 1.1 μm-1,3 μm range (68). Another alternative for the development of integrated photodetectors is the growth of Ge or III-V materials on Si for use as emitters and detectors. The optical properties of such materials are suitable for use in the 0.8 μm to 1.1 μm range. Luryi et al. report the development of a Ge detector on a Si device which can be used as an efficient photodetector for wavelengths of up to 1.5 μm (70).

VI. SUMMARY.

In this work the use of p-n structures as photodetectors in silicon integrated circuits was evaluated. The development of silicon integrated circuits with integrated photodetectors is of interest as they offer the possibility of creating optically testable and optically interconnected devices. Optical inputs located at various positions in an integrated circuit would offer great advantages over current technologies employing input pads and bond wires which are limited in number and constrained in position to the periphery of the chip.

A digital complementary metal-oxide-semiconductor (CMOS) device was used as a test vehicle. Five structures were identified for use as photodetector;: three p-n junctions which can be used as photodiodes, one n-p-n phototransistor, and one photodiode-transistor configuration. These structures are fabricated in the CMOS process and similar structures are fabricated in other technologies.

The spectral responses of the p-n structures were modeled by dividing the device into several regions and solving the diffusion equations which describe the minority carrier density. Measurements were then made to determine the actual spectral and temporal responses, along with the peak responsivity. All of the structures were found to have spectral responses which decreased rapidly above 0.8 μm. This was predicted correctly for one of the p-n structures but the models used did not accurately predict the spectral responses of the other p-n structures. It was postulated that electric field effects due to the substrate doping profile need to be taken into account for accurate modeling. The temporal responses of the structures were studied with the predicted minimum rise times found to be 10 ns or less for the p-n structures and 500-1000 ns for the phototransistor and photodiode-transistor structures. The peak responsivities of the p-n structures ranged from 0.42 to 0.49 A/W as measured using a laser in the spot mode.

The characteristics of the structures studied indicate that they can serve as adequate photodetectors but only over a limited spectral range. Using lasers in the 0.4 μm to 0.7 μm range, it is possible to generate sufficient current to change the logic state of a CMOS inverter. Laser testing of integrated circuits is thus possible. The low responsivities of the structures above 0.8 μm will severely limit their usefulness as photodetectors in optical systems in the 0.8 μm to 1.3 μm range. The temporal responses of the structures, along with the circuit configuration, limit the maximum frequency at which the structures can be modulated.

This work provides information which may be useful in developing integrated optoelectronic systems. The models used to describe the spectral responses of the structures need to be enhanced to include electric field effects due to doping density distributions. This would enable the accurate prediction of the spectral responses of p-n junctions fabricated in various technologies. By controlling process parameters such as doping profile and junction depth, it would be possible to fabricate integrated photodetectors with spectral responses that are optimized for a particular wavelength. The information in this work is also useful for comparing the potential for use of p-n junction photodetectors with other integrated photodetectors including photoconductive elements and Ge or III-V detectors grown on silicon.

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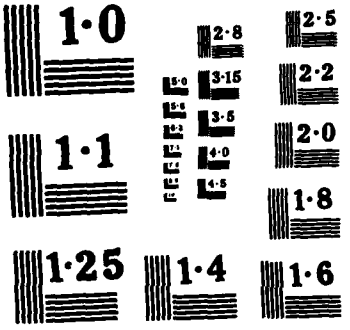
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